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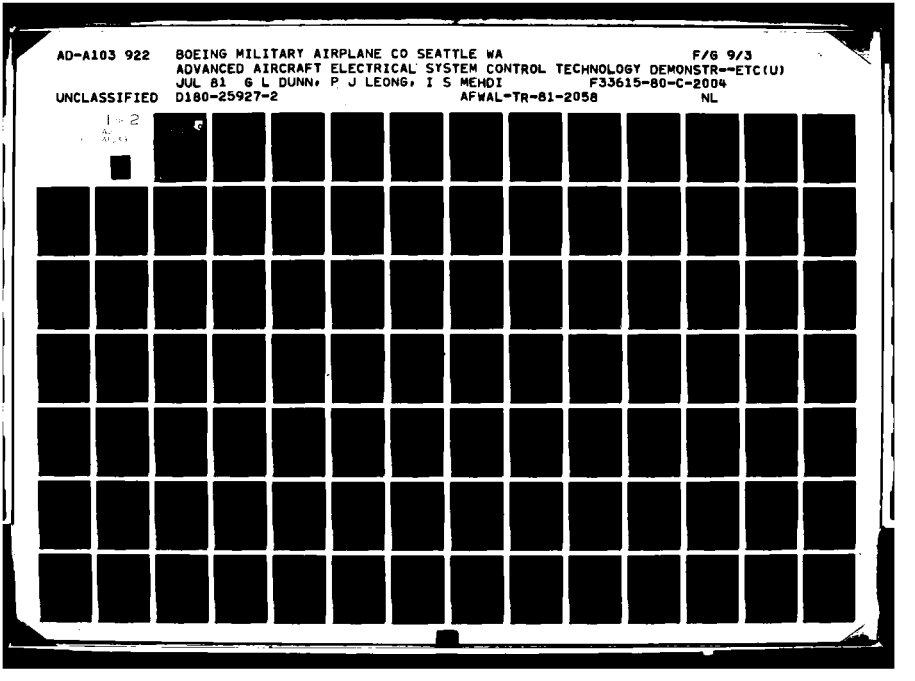

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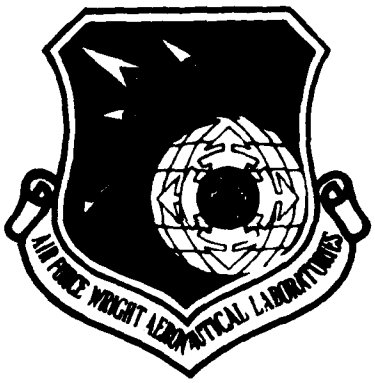

ADVANCED AIRCRAFT ELECTRICAL SYSTEM CONTROL TECHNOLOGY DEMONSTRATOR
- Phase I: Requirements Analysis & Conceptual Design

G. L. Dunn
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BOEING MILITARY AIRPLANE COMPANY
SEATTLE, WASHINGTON

JULY 1981

INTERIM REPORT FOR THE PERIOD SEPTEMBER 1980 TO FEBRUARY 1981

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This technical report has been reviewed and is approved for publication.

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Load Management
Remote Terminal (RT)
Solid State Power Controller (SSPC)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report documents the results of Tasks 1 and 2, Phase I, of this two phase program. In Task 1, the requirements for the electrical power system and the integrated power system control were defined. In Task 2, three conceptual designs for the electrical power system were prepared. Each design incorporated a different data bus architecture, integrated, hierarchical, and non-integrated dedicated. The three designs were evaluated for application to a two engine tactical aircraft. Processor and data bus loading were examined for each architecture. Based on the evaluation, the conceptual design based on the

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20. ABSTRACT (Continued)
integrated architecture is recommended for preliminary design in Task 3, Phase I.

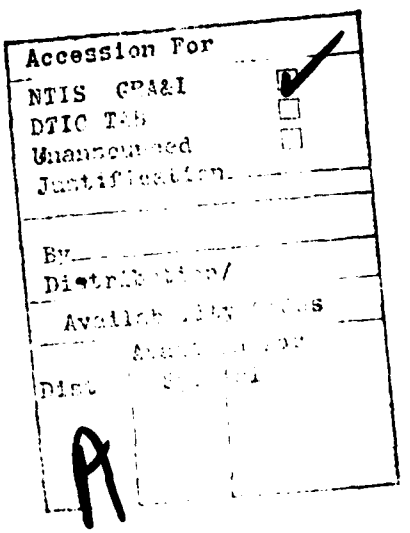
PREFACE

This Interim Technical Report presents the results of work performed by the Boeing Military Airplane Company, Seattle, Washingtion, under Air Force Contract F33615-80-C-2004, during the period from September 1980 to February 1981. The work was sponsored by the Aero Propulsion Laboratory, Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio, under Project 3145, Task 314529, Work Unit 31452959 with Mr. Duane G. Fox, AFWAL/POOS-2, as the project engineer.

The Harris Corporation, Melbourne, Florida and the Eaton Corporation, Milwaukee, Wisconsin were subcontracted to provide information and consultation in the areas of multiplex data bus equipment and solid state power controllers.

This document, which covers Task 1, Requirements Analysis, and Task 2, conceptual Design, of Phase I, fulfills the requirements of CDRL item number 8.

The program manager was I.S. Mehdi. The report was prepared by G.L. Dunn and P.J. Leong who were technically responsible for the work.



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SUMMARY

In this interim technical report, the electrical power generation and distribution requirements for a light tactical aircraft were examined. Two electrical power system configurations which will support fly-by-wire flight control systems were developed. The number of loads, data input/output requirements, generator sizing, and control requirements were determined for the electrical system. In addition the requirements for power management on a tactical two aircraft were determined. Bus loading, processor loading, reliability, computer memory and costs were all examined for both a hierarchical and integrated data bus architecture. The baseline for comparison of there two architecture was a separate dedicated data bus architecture for the electrical power system.

A conceptual design for the above three architectures was performed to meet the power system requirements defined in Task 1. Conceptual designs to the functional block level were provided for the RTs and ELMCs.

The results of the effort conducted in Tasks 1 and 2 indicate that for a light tactical aircraft the distribution and control of the Electrical Power System should be integrated with that of the avionics data bus. This integration is made possible by the use of "smart" ELMCs, which allows the system processor and data bus loading to remain within the design goals of 50% loading.

SECTION I

INTRODUCTION

1. BACKGROUND

The Air Force Wright Aeronautical Laboratories (AFWAL) Aero Propulsion Laboratory has been sponsoring research and development programs directed toward applying advanced solid state power switching and computer control technology to aircraft electrical power systems. Development of components and subsystems utilizing solid state power switching and microprocessor based computer technology has progressed rapidly. Multiplexing techniques have been developed for transmission and processing of electrical system control data. This data usually consists of a large number of discrete (on/off) signals and information for solving control logic equations. Multiplex hardware and software designs have been optimized for electrical system control applications such as the B-1 E-Mux system. This, however, results in high initial development, integration and logistics costs. On large aircraft the amount of signal processing and data transfer may justify the use of a separate and optimized multiplex system for the electrical system control; however, in the case of smaller aircraft this may not be the most cost effective solution.

For small aircraft, where the electrical system signal processing and data transfer may not be as large as for the B-1, it may be possible to integrate electrical system control with the avionics system in a single data bus system as developed in the DAIS program. Previous studies, such as AFAPL-TR-73-41, (Reference 1), examined this concept and concluded that integration was possible. Integration of the electrical power control was also examined in the DAIS program but was not implemented. Areas of concern with such integration are that the electrical power redundancy required for mission essential functions may not be adequate for flight critical functions. Another area of concern is that if the electrical power system is controlled by the multiplex system and in turn the multiplex system requires electrical power to operate, procedures must be devised to power-up the system. The third area of concern is that growth of the data bus traffic may get to the point where the system complexity would negate the technical and cost advantages of an integrated system.

In order to permit evaluation of aircraft electrical power system design, laboratory simulators need to be designed and built. An A-7 electrical system simulator (Reference 2) was built at the Aero Propulsion Laboratory for demonsrtrating the functional operation of the solid state distribution concept and to show that electromagnetic interference (EMI) presented no problem. This simulator was built such that it would have the same ground planes and shielding that exists on the A-7 aircraft. This type of simulator has several disadvantages such as, difficulty in maintenance due to tight hardware locations and difficulty in making changes to the wiring harness, plus the poor utilization of the laboratory floor space.

Modular concepts of building a laboratory simulator (Reference 3) provide the advantages of lower cost, easy modification and more universal application, even though they do not allow for adequate EMI evaluation. To date no simulator has been developed to evaluate an integrated power and avionics data bus.

2. PROGRAM OBJECTIVES

The overall objective of this contract is to develop an aircraft electrical power distribution and control system that is integrated to the fullest practical extent with an aircraft digital avionics information management system (DAIS). Specifically this program has two distinct objectives. They are, first, to define the requirements and conduct the design of a computer controlled, solid state electrical power distribution and control system for a small two engine aircraft, and second to develop the design of a laboratory simulator for the evaluation of the aircraft electrical system.

3. APPROACH

To achieve the objectives of the program, a two phase study with three tasks in Phase I and two tasks in Phase II was undertaken. The tasks for each Phase are as follows:

Phase I Analysis and Preliminary Design
Task 1 Requirements Analysis
Task 2 Conceptual Design
Task 3 Preliminary Design

Phase II Detailed Design
Task 1 System Hardware and Software Design
Task 2 Support Hardware and Software Design

The program flow chart for Phase I is shown in Figure 1. During this phase, in Task 1, the requirements are defined for the electrical power system and the integrated power system control for a small two engine tactical aircraft which will be capable of performing various missions (fighter, attack, reconnaissance, trainer, electronic warefare, fighter bomber). In addition, a data base of information regarding subsystems and component hardware and software of an Advanced Electrical Power Systems (AEPS) Simulator is accumulated. The requirements definition and data base is developed with the primary objective of achieving the most cost effective designs for both the aircraft electrical system and electrical system laboratory simulator. To keep the system cost at a minimum the program is tailored so the requirements meet as closely as possible the existing electrical and DAIS system requirements and applicable hardware and software available at the AFWAL Aero Propulsion and Avionics Laboratories.

In Task 2, each of 3 data bus architectures (single integrated bus, hierarchical integrated bus, separate dedicated/non-integrated bus) are configured with options ranging from all computational capability residing in the digital processor (mission computer) to most of the processing relegated to the Remote Terminals. Based on these options AEPS conceptual designs are prepared. A tabulation of all the relevant parameters including processor/bus loading, reliability, memory, and cost is made. The baseline for the architectural studies is the separate dedicated/non-integrated data bus. Both the hierarchical integrated bus and the single integrated bus are evaluated against this baseline.

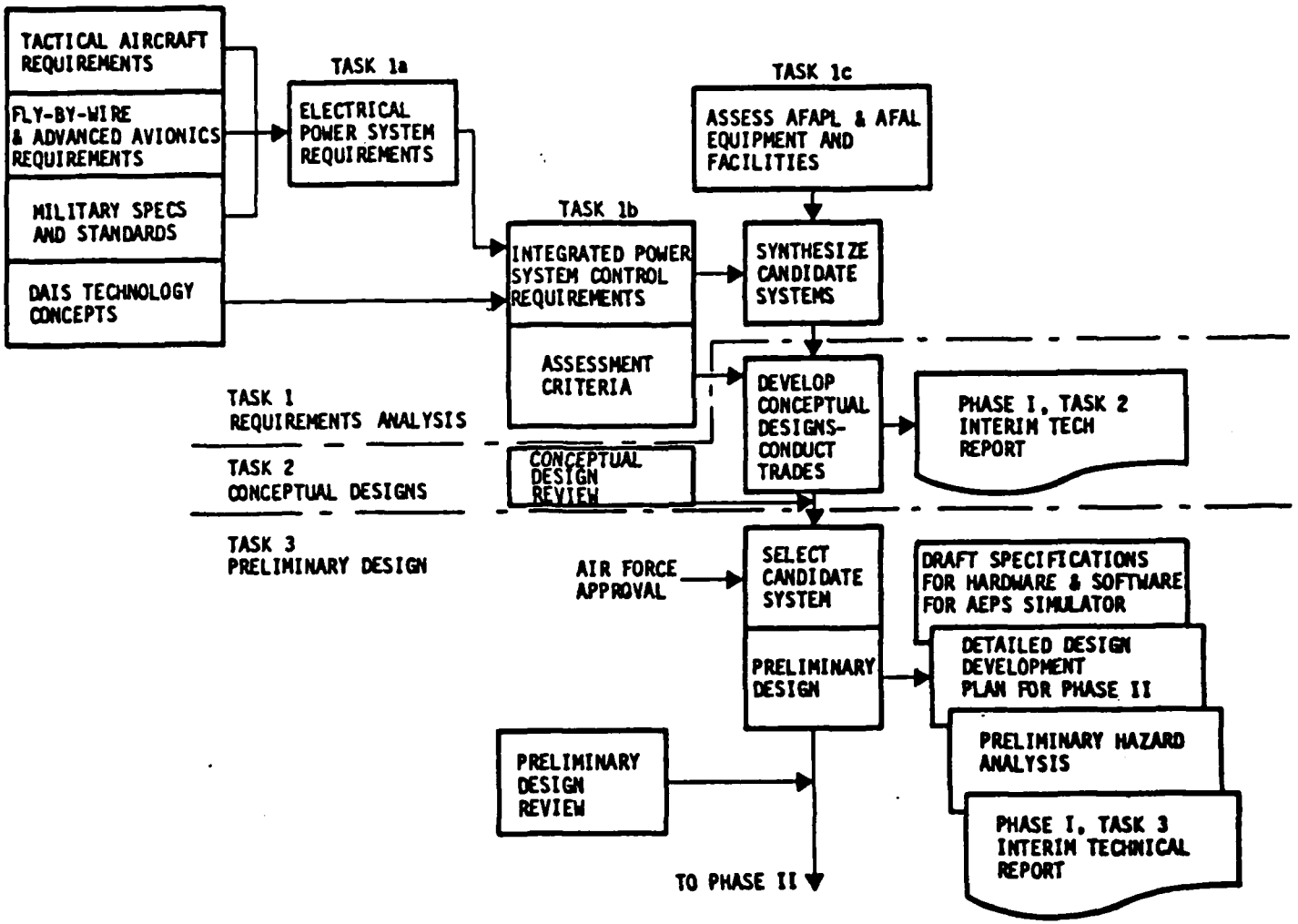


Figure 1 Phase I Program Flow Chart

Also, during Phase I an evaluation of the Aero Propulsion and Avionics Laboratories and equipment is made. This evaluation helps to arrive at a cost effective design of the laboratory simulator through ulilization of existing hardware.

This Interim Technical Report covers results for Phase I, Tasks 1 and 2. Based on the architectural trade studies, one of the three control architectures is recommended for preliminary design.

SECTION II

REQUIREMENTS ANALYSIS

1. ELECTRICAL POWER SYSTEM ANALYSIS

The design options were developed for an electrical power system for a small tactical two engine aircraft with advanced avionics and fly-by-wire (FBW) flight controls. The following assumptions were made to arrive at the electrical system requirements:

- o 2 Engine Driven Generators
- o 1 Flight Operable Auxiliary Generator
- o Mission Completion With 1 Main Generator
- o Safe Return With Auxiliary Generator
- o Triple Redundant Fly-By-Wire Flight Control System
- o FBW Electronics will be Powered by DC Power
- o Solid State Distribution

A primary generator is driven by each engine. The auxiliary generator is driven by a flight operable auxiliary power unit.

The electrical power system requirements include provisions to interface with the following subsystems:

Automatic Flight Control	Hydraulic Power
Auxiliary Power	Instruments
Communications	Landing Gear
Crew Escape	Life Support
Engines	Lighting
Environmental Control	Navigation
Flight Controls	Stores Management
Fuel	

The degree to which each subsystem is interfaced varies. For some subsystems such as automatic flight controls, the interface will be only to provide power and caution and warning indication. For other subsystems, such as environmental control, allocations were made for more extensive interfacing, such as on/off control of equipment and sensor data communication.

a. Electrical System Configuration

(1) Mission Effects

Several aircraft with different missions were surveyed with the intent of determining the effect of the mission on the generation capacity. The survey data is shown in Table 1.

TABLE 1
GENERATION CAPACITY OF EXISTING AIRCRAFT

AIRCRAFT	MISSION	GENERATOR SIZE-KVA	NUMBER OF GENERATORS
F-4C	FIGHTER	30	2
F-5		15	2
F-14A		60/75	2
F-14B		75/90	2
F-15		40/50	2
F-16		40/50	1
F-18		30/40	2
A-4H	ATTACK	20	2
A6-A		30	2
A-10		40	2
EA-6B	ELECTRONIC WARFARE	30	2
		27 KVA POD	1
EF-111A		90	2
FB-111	FIGHTER BOMBER	60	2
T-38	TRAINER	9	2
T-39D		10	2
U-2	RECONNAISSANCE	30	2

The survey shows that the fighter, electronic warfare, and fighter bomber missions required the most power of all the missions. Of the fighter aircraft, the two-man crew F-14B has the largest generation system. This may be attributed to the fact that a two crew member aircraft would contain more sophisticated and power consuming equipment relative to a one crew member aircraft. The electronic warfare mission aircraft have additional generation capacity over similar aircraft without the electronic warfare capability. The EA-6B's two main generators are the same size as the A-6A attack aircraft; however, the EA-6B carries an additional 27 KVA pod mounted ram air turbine driven generator for the additional power required for the electronic warfare equipment. In the case of the EF-111A, the generator size increased from 60 to 90 KVA over the FB-111. The attack, trainer, and reconnaissance missions have low power requirements as shown in Table 1. In this group, the A-10 has the largest generation capacity.

From the survey, it is apparent that the newer aircraft have larger power requirements. Specialized electronic warfare aircraft require additional power over the attack or fighter bomber versions of the same aircraft.

The circuit breaker counts of three aircraft were examined. The number of circuit breakers, along with the generation capacity of each aircraft, are shown in Table 2. The data shows that the number of circuit breakers increased as the generation capacity increased. The ratio of AC and DC circuit breakers was not constant. The FB-111 has more DC than AC circuit breakers. The reverse is true for the other two aircraft.

TABLE 2
CIRCUIT BREAKER ANALYSIS

AIRCRAFT	TOTAL GENERATION CAPACITY	AC	DC	TOTAL
EA-6B	87KVA	174	90	264
F-15A	100KVA	190	131	321
FB-111	120KVA	201	227	428

The trend for new aircraft is toward more electrical power generation capacity. This is the result of increased sophistication in avionics, weapons, and flight control systems. Aircraft dedicated to electronic warfare missions require greater amounts of power. Next to the electronic warfare mission, the fighter and fighter bomber aircraft have the highest power requirements.

The AFAPL-TR-79-2084 (Reference 4) study estimated that about 400 solid state power controllers (SSPCs) would be required for a single engine aircraft. With a one-for-one circuit breaker replacement, 400 SSPCs would meet the requirements for EA-6B and F-15A aircraft. It is recommended that for the AAES Control Technology Demonstrator program the electrical system contain 500 SSPCs. This many SSPCs would cover all missions under consideration, allow for growth, and allow for load complement reconfiguration. With two engines, and two generators, the additional 100 SSPCs will take care of the additional sophistication of a two engine aircraft.

(2) Load Analysis

A load analysis for a two engine tactical aircraft was developed. The analysis is based on the air-to-surface fighter which Boeing is studying. The load analysis encompasses the fighter and fighter-bomber missions and also has some ECM capabability, though not to the extent of the EF-111 or the EA-6B. A load profile developed from the analysis is shown in Figure 2. The load analysis is summarized in Table 3.

TABLE 3
ELECTRICAL LOAD ANALYSIS SUMMARY

	MAXIMUM CONNECTED LOAD	SUSTAINED PEAK EMERGENCY LOAD
TOTAL AC POWER	58477 VA	12577 VA
TOTAL DC POWER	7805 WATTS	2630 WATTS
TRU LOSSES	1377 WATTS	465 WATTS
TOTAL TRU INPUT POWER	9182 WATTS	3095 WATTS
TOTAL AC AND DC POWER	67659 VA	15672 VA

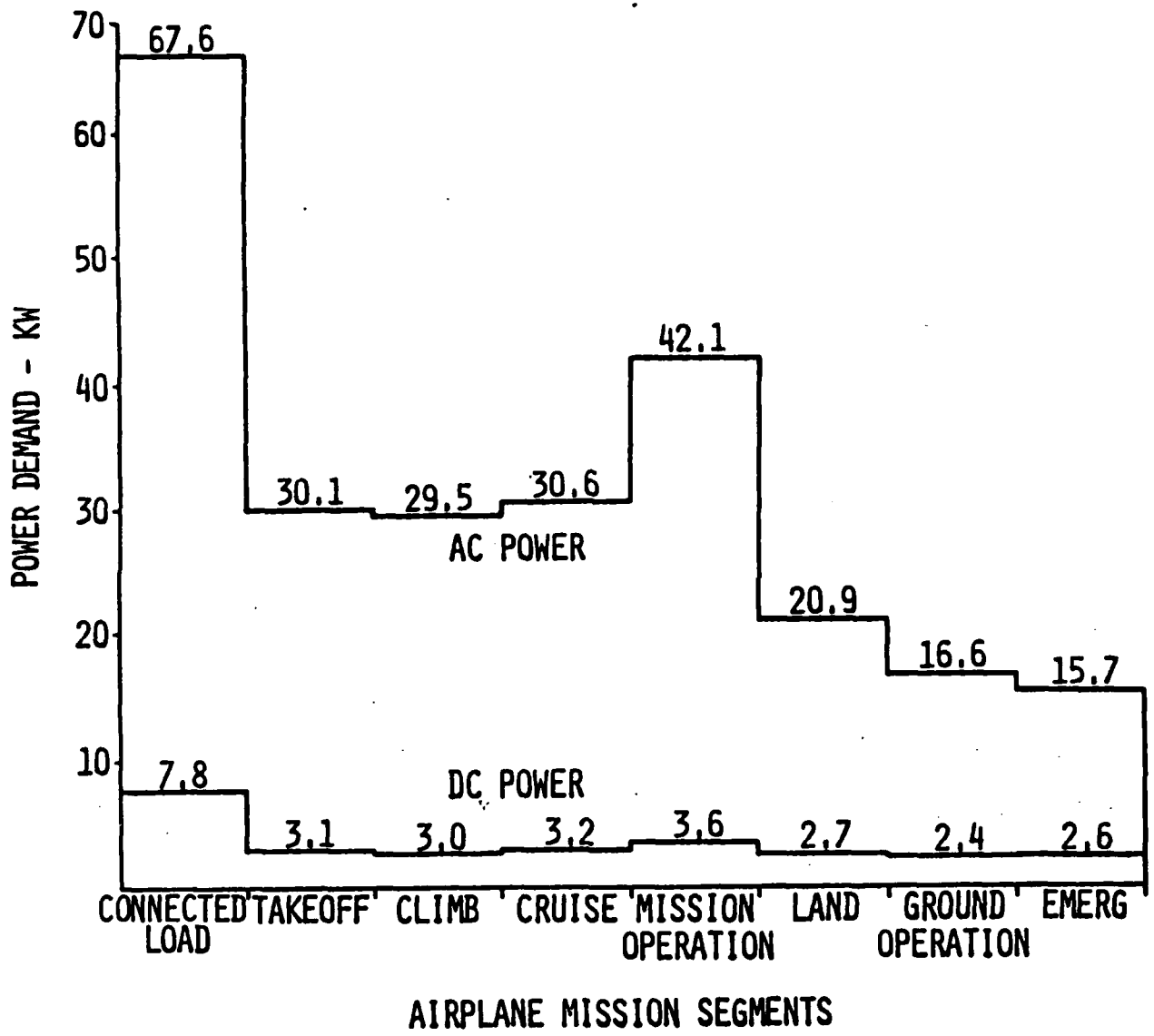


Figure 2 Electrical Load Profile

(3) Generation Complement

Using the load analysis and the mission effects analysis as a base, the generation and distribution system was sized. The generation system complement is shown below.

2-60 KVA 115 VAC Generators
1-20 KVA 115 VAC Auxiliary Generator
3-100 Amp 28 VDC Transformer Rectifier Units

Two 60 KVA main generators allow mission completion with one generator out. Three 100 amp transformer-rectifier units (TRU) provide the system's DC power. The TRUs are sized to provide power for all connected loads. Two TRUs will provide enough DC power for mission completion.

(4) SSPC/ELMC Interfacing Requirements

The majority of the SSPCs will be packaged on printed circuit cards in the electrical load management centers (ELMC). The interface between the electrical control system and the SSPCs was analyzed. These signals, for the control and monitoring of the SSPCs, were chosen:

- o On/Off Control - signal to turn the SSPC on and off.
- o Trip - indicates that the SSPC has tripped due to an overload.
- o Status - indicates whether or not the SSPC output is high, independent of the on/off control signal.

The status signal is used as a built-in-test (BIT) function for the SSPC. The status signal is compared with the control signal to see if the output is in agreement with the input signal. A disagreement indicates a SSPC failure.

Three ways for transmitting these signals are shown below:

- o 6 wires - one pair of wires for each signal.

- o 4 wires - one signal wire for each signal with a common return.

- o 2 wires - all three signals are transferred over a single pair of wires. The ON signal is supplied as a constant current source between 3 and 10 milliamperes. TRIP and STATUS are represented by different preselected input impedances, looking into the SSPC control terminals. The voltage across the control input is measured to determine TRIP and STATUS.

The 4 wire method was selected for interfacing the SSPCs. In an ELMC, the wire lengths are short. The advantage of having only two control wires to each SSPC is thus minimized by the simpler control circuitry required for the 4 wire method. The advantage of the 6 wire method is better noise immunity over the 4 wire method; however, the wire runs in the ELMC are minimum and the ELMC enclosure provides shielding from EMI.

(5) SSPC Distribution

Five hundred SSPCs will be used to distribute power to aircraft loads. A distribution of the 500 SSPCs has been developed and is shown in Table 4. To develop this list, the detailed load list provided in Appendix A of Reference 5, was proportionately reduced in power and modified to reflect the analysis of Appendix B of Reference 5, and the single engine analysis in Reference 4. Loads requiring SSPCs larger than 7.5A AC or 20A DC will be controlled by discretely packaged SSPCs or electromechanical power controllers located outside of the ELMCs.

TABLE 4
SOLID STATE POWER CONTROLLER DISTRIBUTION

115 VAC

SIZE	PERCENT TOTAL
2A	31.5
3A	8.5
5A	7
7.5A	3

28 VDC

SIZE	PERCENT TOTAL
2A	37
3A	6.5
5A	2
7.5A	2
10A	1.5
15A	.5
20A	.5

(6) Distribution System

The distribution system consists of distributed load centers called electrical load management centers (ELMC). Previous studies (References 4, 5) have shown that this distributed concept lowers vulnerability to combat damage and in some cases lowers total system weight when compared to a single centralized distribution center. The individual loads are connected to the ELMCs rather than to the main electrical power buses as in conventional electrical systems. Power to the loads are controlled by SSPCs housed in the ELMC.

For a single engine fighter, (Reference 4) 5 ELMCs were recommended. The two engine tactical aircraft of this study is in the same size category. 5 ELMCs provide coverage for the whole aircraft. The locations of the ELMCs are shown in Figure 3. The main distribution center consists of the main AC and DC buses which are connected to the generators and TRUs.

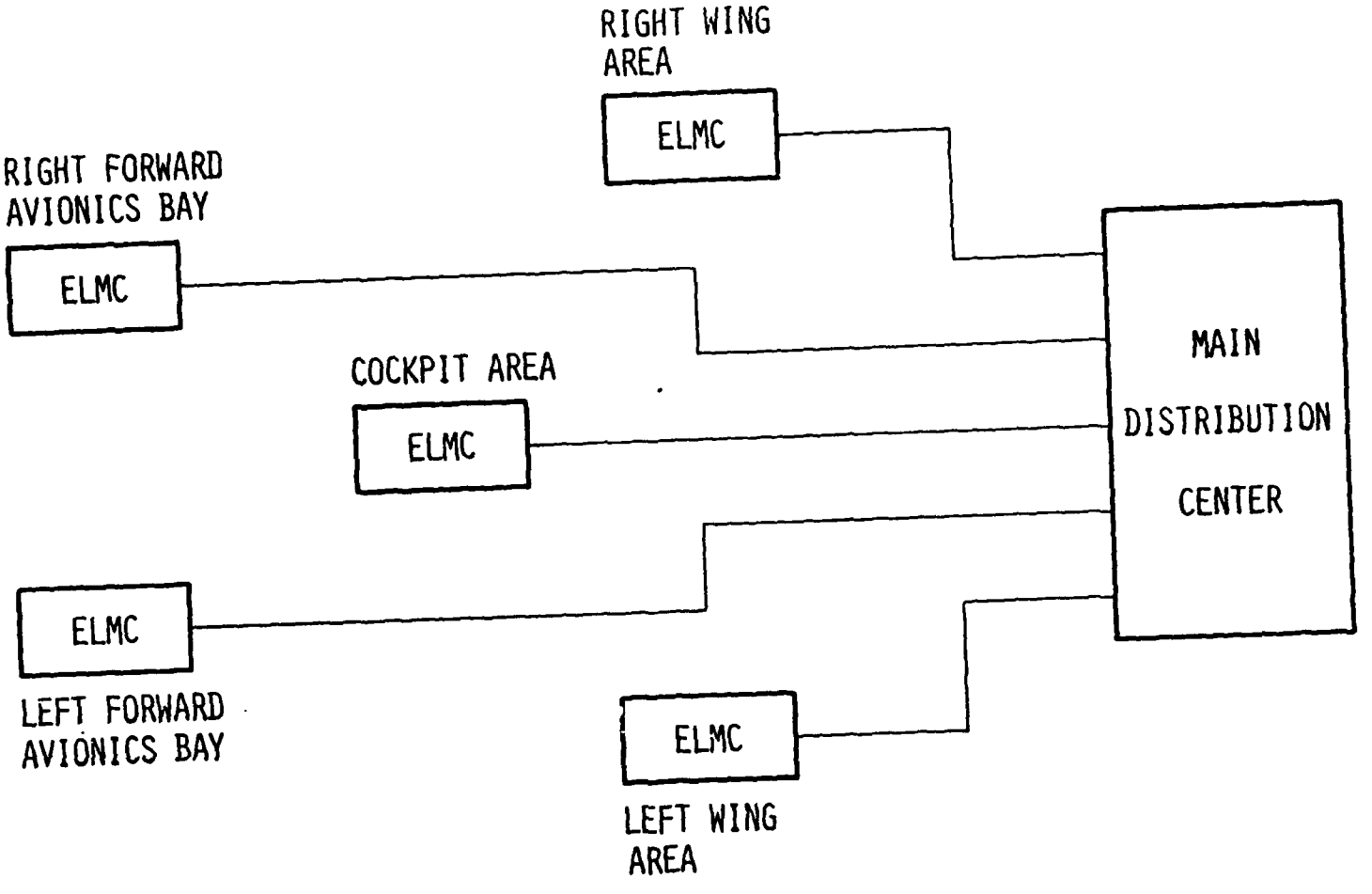


Figure 3 ELMC Locations

The primary functions of the ELMC are to house the SSPCs and interface the SSPC to the data bus. To maximize the utility of each box on the data bus, the ELMC will include additional functions such as those incorporated in remote terminals (RT). This will keep the number of boxes on the data bus at a minimum. The additional capabilities which will be included in the ELMC are analog-to-digital (A/D) conversion and discrete input/output (I/O).

The ELMCs handle 15% of the system's discrete I/O data transfer. Remote terminals handle 80% of the discrete I/O data transfer and the remaining 5% is allocated to the generator control units. Preliminary design of a remote terminal indicates a capacity of approximately 250 inputs and 118 outputs can be packaged in a 1/2 ATR size box. Based on such a design, three remote terminals are required to handle the I/O requirements of the system.

(7) Flight Critical Power

Methods of providing power to flight critical equipment were investigated. In particular, ways of providing power to a triple redundant fly-by-wire flight control system were addressed. Two types of power are available, AC and DC. Both were evaluated for the application. Table 5 lists the ways the flight critical power requirements are met using AC or DC power.

TABLE 5
FLIGHT CRITICAL POWER

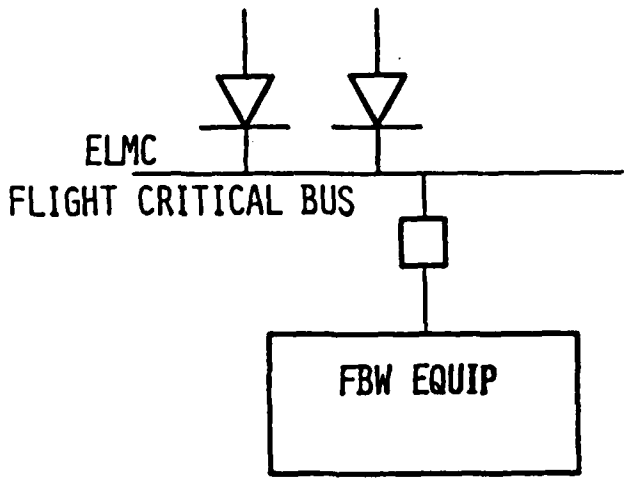
REQUIREMENTS	DC POWER	AC POWER
3 ACTIVE SOURCES	3 TRUS	2 AC GENERATORS AND 1 INVERTER
UNINTERRUPTIBLE POWER	DIODE PARALLELING	COMPLEX DESIGN
SHORT TERM EMERGENCY	BATTERY	BATTERY THRU INVERTER
LONG TERM EMERGENCY	AUXILIARY GENERATOR THRU TRU	AUXILIARY GENERATOR

As a design philosophy, each channel of the flight control system must have its own independent power source. These sources may be cross tied for additional redundancy. For a triple redundant flight control system, three independent power sources are thus required. With DC, this provision is easily met by using three TRUs. With AC, the main generators provide two sources. A third source can be an inverter powered from a DC bus. A drawback to using AC power is the lack of a simple method for providing uninterruptible power to the flight critical equipment. With DC power, this is accomplished by diode paralleling the sources.

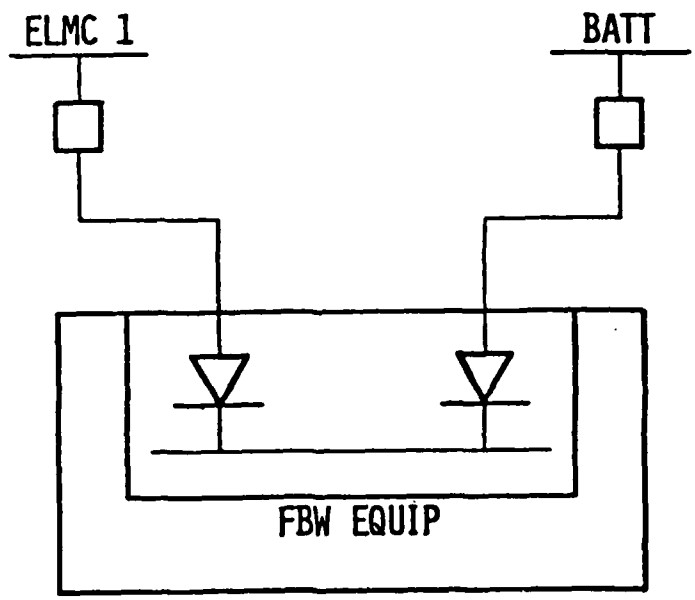
DC power is recommended for the flight critical systems. Two concepts were developed for providing power to flight critical equipment, in particular the fly-by-wire flight control electronics. In the first concept (Figure 4a), a Flight Critical Bus is provided in the ELMC. Each bus is powered by its own TRU. Backup power is provided by a battery which is paralleled with the TRU. Any number of flight critical equipment can be connected to the bus; however, where redundancy is required, such as a triple redundant flight control system, only one channel of equipment is connected to each bus. In the second concept (Figure 4b), no special bus is provided in the ELMCs. The flight critical equipment is connected to the normal DC bus within the ELMC. Redundant equipment is connected to different ELMCs. Battery power for backup is provided directly to the equipment. The first concept is recommended for this study. Having a flight critical bus in the ELMC provides more versatility and reduces the number of load feeders. The vulnerability of the load due to the single feeder is minimized by short feeder lengths resulting from having 5 ELMCs distributed throughout the aircraft.

(8) Power Bus Configuration

Two electrical power bus configuration have been developed. Both configurations have provisions to support fly-by-wire flight control systems. The two configurations, A and B, are shown in Figures 5 and 6. Only three of the five ELMCs are shown. The advantages and disadvantages of each configuration are discussed below.



a. Flight Critical Bus in the ELMC



b. Dual Source of Power to FBW Equipment Terminals

Figure 4 Power Delivery Concepts for Flight Critical Equipment

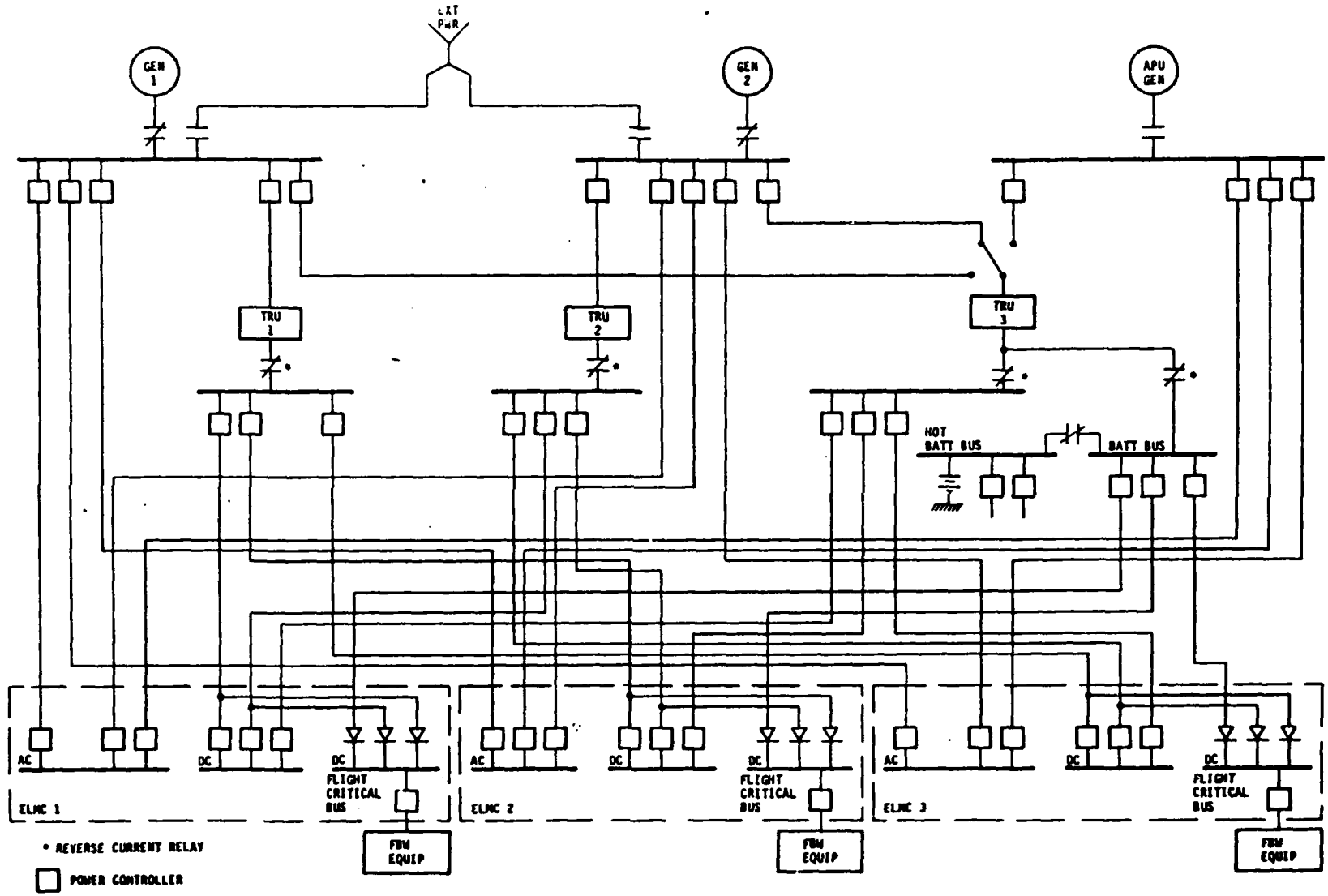


Figure 5 Power Bus Configuration A

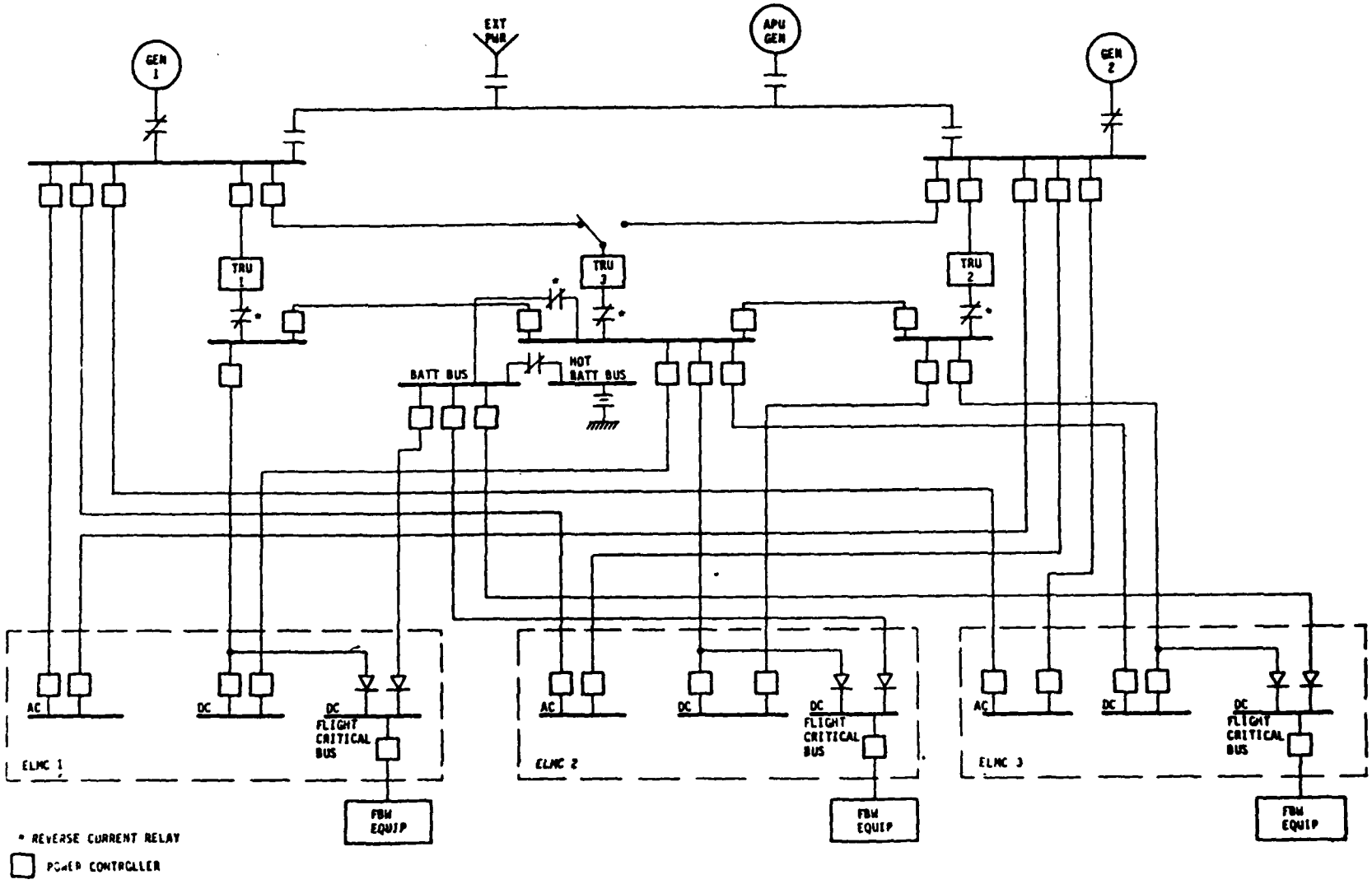


Figure 6 Power Bus Configuration B

Configuration A: This configuration provides maximum isolation of power sources. Each power source has its own bus and its own power feeder to each ELMC. A fault on one bus will not affect the other buses. The disadvantage to the configuration is the increased wiring, switching devices, and protective devices required over configuration B. Since power feeders cannot be shared by the power sources, each ELMC has three sets of 3 AC feeders and three DC feeders.

Configuration B: Bus ties are incorporated in this configuration. In the AC system, the bus ties eliminates the need for separate power feeders for the auxiliary generator. The auxiliary generator supplies power to the ELMCs through the main generator buses. The DC bus ties allows the TRUs to be paralleled and to share power feeders. A disadvantage of this configuration is the additional protection required for the bus ties. Another disadvantage is the dependency of the auxiliary generator on the main generator buses for distributing power. For example, a fault on one of the two main generator buses prevents the use of the auxiliary generator if the unfaulted channel's generator is operating. This happens because the auxiliary and main generator can not be paralleled.

The basic trade off between configuration A and B is additional survivability versus simplicity. The simplicity of configuration B translates to less wiring and, thus, less weight. Since adequate survivability is designed into both configurations, especially for the flight critical loads, configuration B was selected for the conceptual design.

b. System Control And Protection

The system control and protection provides for automatic operation and coordinated fault isolation. Control and protection is sectionalized into the following areas: generator, distribution, and loads. The objectives of control and protection is to:

- o Reduce crew work load
- o Increase flexibility
- o Increase survivability
- o Increase probability of mission success

The reduced crew work load is achieved by automation. The use of digital processors and data bus communication lines link the various subsystems and allow coordination of most of the components of the electrical system with other aircraft subsystems.

Flexibility is achieved by programmable digital processors which control the system. The processors control the individual SSPCs. The capability to reconfigure the system greatly enhances system flexibility.

Increased survivability and probability of mission success are achieved by coordination of all electrical functions and a comprehensive load management program. Automatic switching provides for fast fault isolation, bus switching, and load shedding. Load management diverts power to flight and mission essential loads in the event of a decrease in available power.

Generator control and protection functions have become fairly standardized, with only the threshold levels varying from program to program. The control and protection functions for the generator are shown below. The same functions will be applied to the APU generator.

Generator Protection

- o over/under frequency
- o open phase
- o differential protection
- o over/under voltage
- o input underspeed
- o failed rotating rectifier

Generator Control

- o voltage regulation
- o frequency regulation
- o generator contactor

For advanced aircraft which depend on electrical power for mission completion and flight control, protection and control of the primary generating system is critical. To provide maximum fault isolation and to provide the necessary response time for the control of an aircraft generator, the control and

protection of the generator is accomplished by the generator control unit (GCU) and is not delegated to the system processors. The control and sensor lines to the generator are hardwired. The GCU is connected to the data bus; however, the generator control and protection functions operate independent of any data bus service functions. This isolates the generator from data bus failures. The data bus is used to carry data such as overload instructions, maintenance information, and fault indications, between the GCU and the system processors. Having the GCU hardwired to the generator also facilitates system startup from a "dead" airplane. In addition, loads necessary during startup are controlled by SSPCs which are in the closed state when no control signal is present.

The distribution system includes the main buses, external power receptacles and distribution feeders. The function of the distribution protection system is mainly to provide fault isolation. The protection and control functions associated with the distribution system are shown below.

Protection

- o fault protection and isolation
- o abnormal external power protection

Control

- o bus tie breaker control
- o external power breaker control
- o power distribution to ELMCs

The versatility and survivability of the aircraft is enhanced with the multiplexed data bus control of the loads. All loads are under system control and the status of the loads are constantly monitored. Load control is accomplished by the solution of Boolean control equations. There is one equation for each load. The equation takes the form shown below.

$$C = \bar{L}\ P\ (R + Q)$$

C = SSPC On/Off Control Signal
L = Trip Latch
P = Priority Signal
R = Request for Power (Solution of a Boolean Equation)
Q = Test Request (Such as Ground Test)

The variable R is the output of a system equation consisting of inputs from the system's RTs and ELMCs. The priority signal, P, is used to implement load management. Sixteen load management levels are available. Each level represents a different set of priority signals for the SSPCs. At each level, each SSPC will have an assigned priority, P. A P set to "0" inhibits or commands the SSPC to turn off. A "1" allows the SSPC to turn on. The relationship of the P variable and the load management levels can be visualized as a 16 x 500 matrix (500 SSPCs in the system) of "1s" and "0s." Depending on the load management level implemented, a preselected combination of 500 "1s" and "0s" are substituted for the variable P in the SSPC control equations. The load management matrix is shown in Figure 7. Various system parameters are used to logically select one of the sixteen load management levels. The level can also be selected manually. Figure 8 shows parameters which are used in determining the load management level.

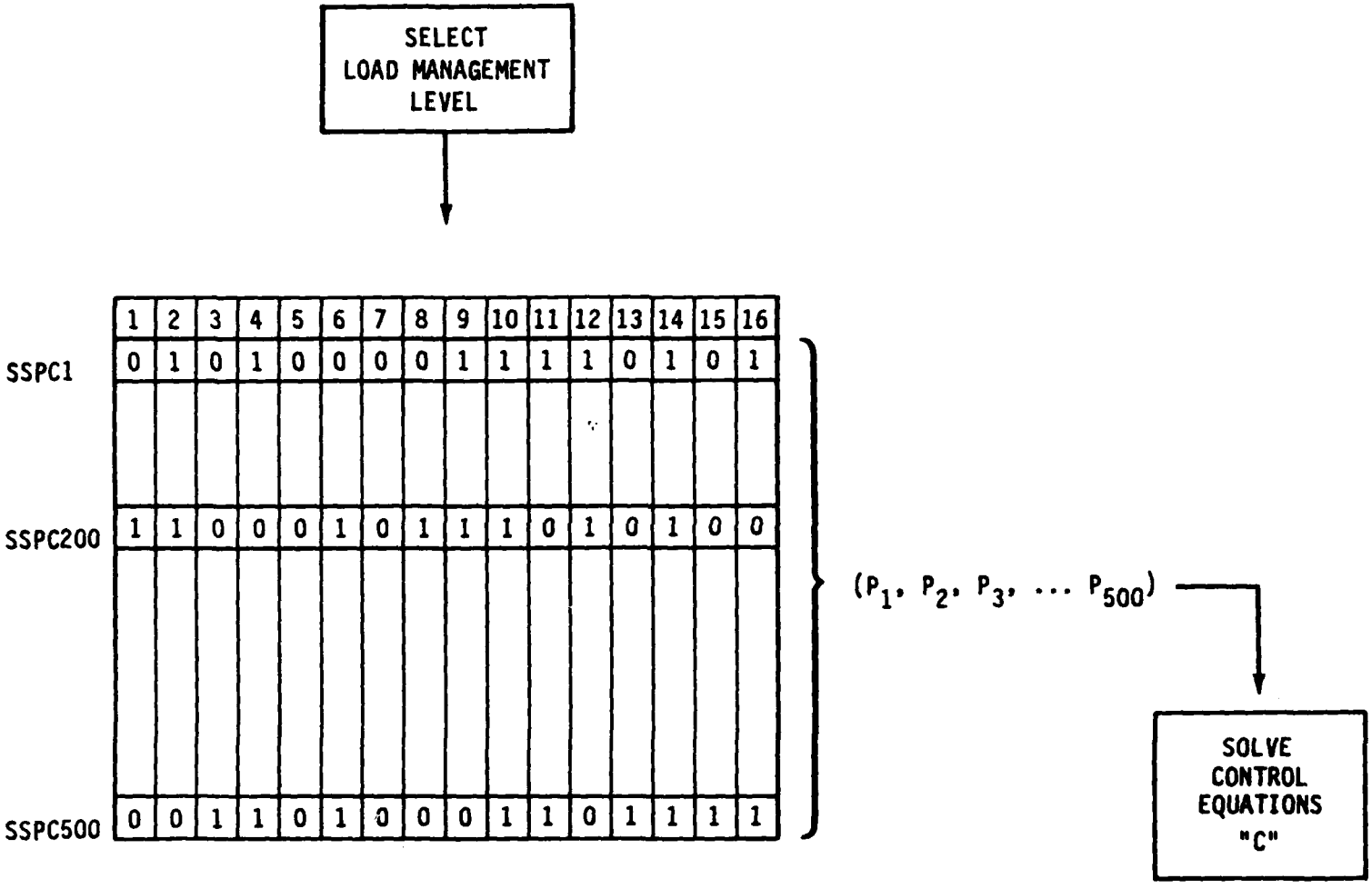


Figure 7 Priority Signal Selection

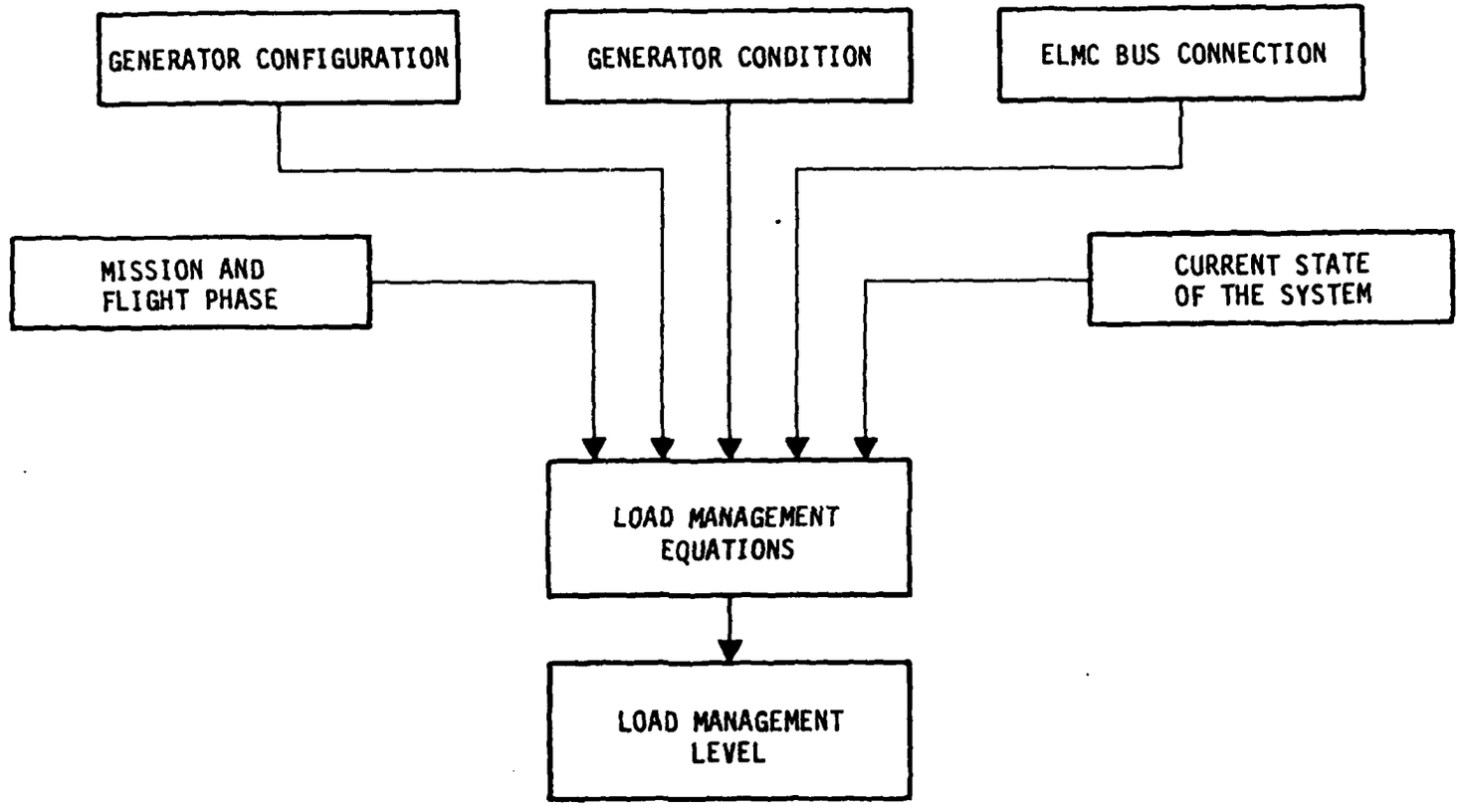


Figure 8 Load Management Level Selection

c. Applicability of J73/I (JOVIAL)

The evaluation of the applicability of JOVIAL higher order language to electrical systems followed two paths. The first was a literature search aimed at a comparison of the efficiency of assembly and higher order languages. The second evaluation path was the actual coding of two typical power control routines in both JOVIAL and assembly language with a comparison of the results. The analyses were performed using J73/I; however, J73/I has since been superceded by J73. The changes made in the language have been in the area of syntax and data type conversion. Also, a few new functions have been added. The differences between J73/I and J73 are minor and do not affect the results of the analyses below. Based on these results, it is recommended that J73 be used as the programming language.

(1) Literature Survey

A survey of current literature has produced the following data to be considered when analyzing the question of using an assembly language or a higher order language.

Assembly language is to date the most efficient method for: accessing certain hardware characteristics of a machine, utilizing minimum amounts of memory, high computational speeds, and input and output capabilities with particular peripherals (References 6,7,9,12). Higher order languages are not yet capable of completely supplanting the assembly language, because of their machine independency. Certain hardware characteristics must still be accomplished utilizing assembly language routines called from higher order language routines.

The trade-off involves determination of whether the amount of memory space and computation time saved by programming in assembly language, justifies the added time, expense, and machine dependency (References 7,9).

Higher order languages have significant advantages over assembly languages (References 6-13):

- o Ease of learning
- o Support Top-Down Structure
- o Support effective problem solving
- o Readability of large programs
- o Support transportability and maintainability
- o Flexibility of data types
- o Higher programmer efficiency
- o Smooth transfer of software responsibility to new personnel
- o Updates create minimal impact on total system
- o Allow focus on problem solving rather than the idiosyncracies of the machine
- o Machine independent

The Air Force has conducted recent studies into the efficiency of the JOVIAL-73/I compiler for producing object code and found that it is within 10% to 15% as "efficient" as comparable assembly language code. In one study two algorithms were selected as representative of an airborne processing problem. One was a mathematical routine which emphasized algebraic computations; the second was a message processing routine that required extensive logic, bit extraction, and partial word manipulation. The results for both routines were similar - the Jovial compiler code required approximately 11% more memory space and ran 10% slower (Reference 10). This decrease in processing efficiency was counterbalanced by greatly increased programming efficiency (i.e., decreased programmer time) by a factor of 2 to 1 (Reference 10,11).

Other studies have shown an increase in programmer efficiency as high as 2.5 or 3 to 1 (Reference 7,10,11,12). Software development time and maintainability time is reduced by a factor of 2 (Reference 12). "High-level languages are to assembly language programming what integrated circuits are to discrete logic - they collect small related elements into neat modules. The benefits too, are similar. Just as the hardware designer needs fewer components to build a system, the programmer thinking in a high-level language needs fewer lines of code to make a system 'go'" (Reference 6).

(2) Evaluation of Higher Order Language Vs Assembly Language by Example

Two routines, OVPROT and GCBCON, shown in Figures 9 and 10, were coded in both J73/I higher order language and 1750 assembly language. These routines were developed for a microprocessor generator control unit. OVPROT is the routine which does the over voltage protection and GCBCON is the routine which controls the generator circuit breaker. The J73/I source code was compiled into the 1750 instruction set. The resulting 1750 compilation of J73/I and the 1750 source code were compared in the following areas:

1) number of instructions
2) memory required. This is memory for executable statements only. It does not include data memory requirements which are assumed to be identical for both J73/I and 1750.
3) execution time
4) programming time. This is the time required to code the routine from a structured flow chart, enter the source lines into the computer and produce an error free compilation or assembly.

The results of this comparison are shown in Table 6. These results agree with the findings of the literature search. The number of instructions decreased by about 11% with the use of assembly language, but the memory requirements stayed about the same. This apparent contradiction is a result of the compiler using many single word instructions while the assembly language coder used several two word instructions. The execution time of the routines drops about 10% when assembly language is used.

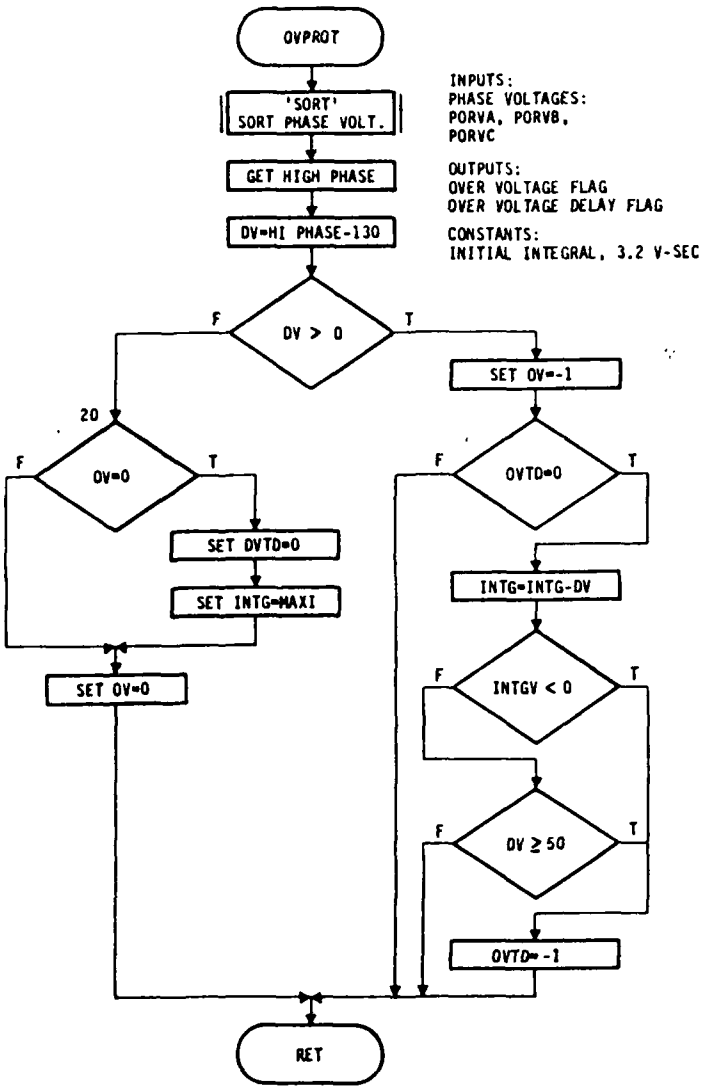


Figure 9 OVPROT Routine

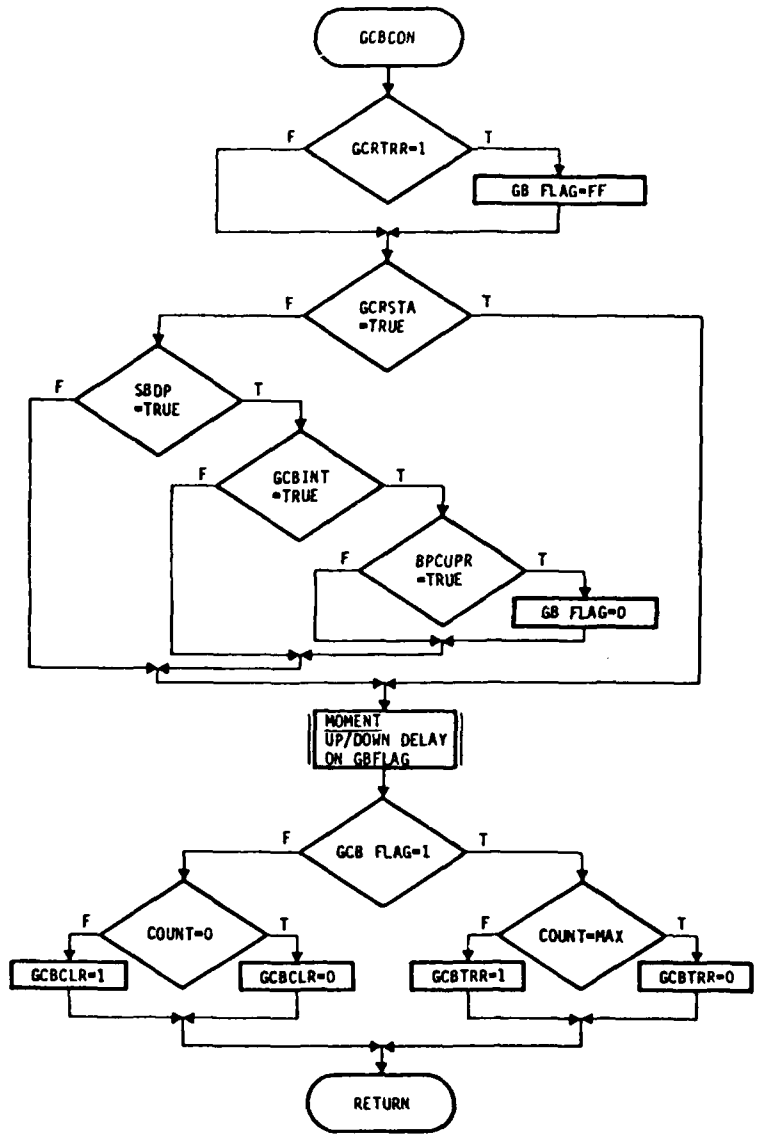


Figure 10 GCBCON Routine

TABLE 6

HIGHER ORDER LANGUAGE STUDY RESULTS

	GCBCON J-73/I	CCBCON 1750 Assembly	OVPROT J-73/I	OVPRCT 1750 Assembly
Time (Code, Type, Compile/Assemble)	1:15 hrs.	2 hrs.	1:45 hrs	2 hrs
No. Of Instructions	33	30	45	39
memory (Does not include data).	51 words	49 words	53 words	54 words
Execution Time	54.25 usec	50.75 usec	79 usec	69 usec

2. INTEGRATED POWER SYSTEM CONTROL

a. Requirements

Processing, bus loading, and response time requirements are defined in this section. Following are the major assumptions for defining the requirements for the integrated power system control:

a) Maximum use of Digital Avionics Information System (DAIS) concepts (Reference 14)

- MIL-STD-1553B multiplexed data bus
- Remote Terminals (RTs) per specification SA-321301
- DAIS executive with synchronous bus protocol
- Use of Jovial higher order language (HOL) for power system application software

b) Separate AN/AYK-15A processor for power system control.

c) Hardware connected to the 1553B bus.

- 5 ELMCs with 100 SSPCs each
- 3 Power system RTs
- 2 Generator Control Units (GCUs)

(1) Processing

Processing requirements for the power system were based on the B-1 EMUX specification (Reference 15). Using the number of SSPCs as a complexity measure, the number and type of equations necessary for the power system in a tactical fighter was determined by scaling the equation count for the B-1 aircraft by the ratio of the SSPC requirement for the fighter to that required in the case of the B-1 EMUX. For example, the EMUX system required 720 SSPCs for each data bus. Our analysis of the power system established a requirement of 500 SSPCs. Therefore, a B-1 EMUX requirement for 300 one variable equations results in a (500/720) x (300) = 208 one variable equation requirement for the two engine tactical aircraft power system.

The processing requirements can be separated into three categories of equations as described below.

Category I: These are power request equations and are of the form Z=R where R may take one of the following forms:

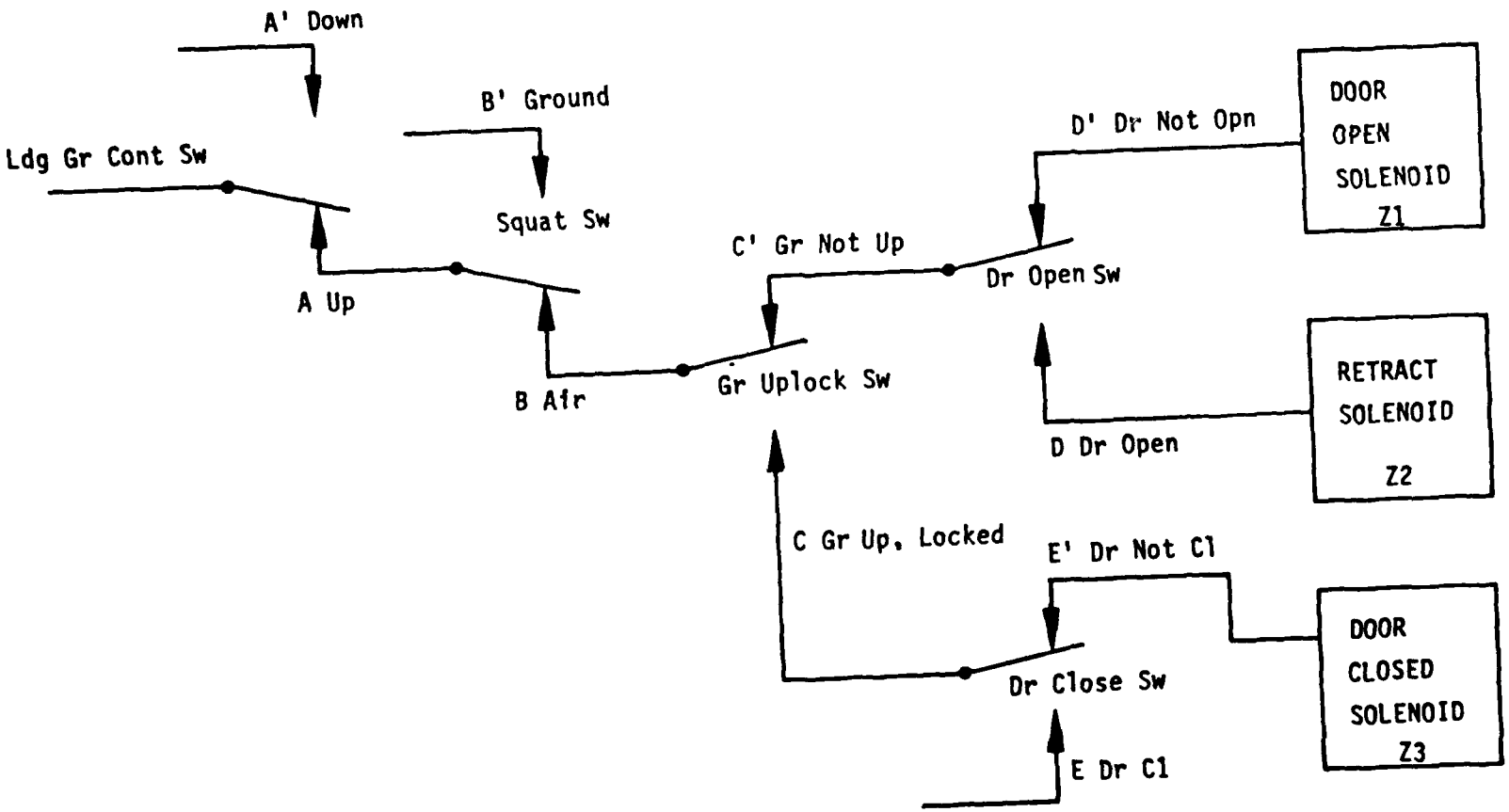
Form 1	One variable of the form A or $\bar{A}$, or the value "logic 1"
Form 2	Five variables arranged in any valid Boolean expression with each variable used once, only
Form 3	Twenty variables arranged in any valid Boolean expresson with each variable used once, only
Form 4	Two hundred variables arranged as the sum of products with each product term composed of no more than six variables with no variable repeated in the Boolean expression

There will be 208 form 1, 236 form 2, 45 form 3, and 8 form 4 equations for this aircraft. Figure 11 shows an example of how typical Category I power request equations would be derived from various airplane discretes.

Category II. There are 500 SSPC power control equations of the form:

$$C = \bar{L}P\ (R + Q)$$

Where R is a Boolean expression of Form 1, 2, 3 or 4 listed above; P is a single variable; L is the solution to the latch equation and Q is test request.



A = Landing Gear Handle UP
B = Air Vehicle Airborne
C' = Landing Gear Not UP
D' = Door Not Open
E' = Door Not Closed

A1 = A•B•C'•D' Energizes door open solenoid
Z2 = A•B•C'•D' Energizes gear retract solenoid
Z3 = A•B•C •E' Energizes door close solenoid

where Z = the summation, result or response
and • = "and" (rather than "or")

Figure 11. Discrete Data Processing Example

Category III. There are 500 power system status equations of the form:

$$I = (L + PX)$$

Where L is as defined in Category II above; P, and X are single variables available to the system designer for definition.

(2) Input/Output Requirements

In the power system, the input/output consists of the data and traffic transmitted between the power system processor and its ELMCs and RT in order to accomplish the power system management and control functions. The input/output requirements were determined by scaling the B-1 EMUX requirements by the ratio of the SSPC count. The discretes transmitted on the bus consists of sensor, SSPC status, system control and status, RT sync, and mode control information.

The B-1 EMUX specification has a total of 2768 discrete inputs. To this were added one discrete per digital serial word from the avionics subsystem. Since 249 words are possible, 249 discretes were added to the total. Scaling these requirements results in a total of 2096 discrete inputs for this study. Similar scaling of the EMUX outputs results in a data bus traffic loading of 1041. It was assumed that the GCU interface with the power processor would require approximately 50 descretes for either input or output. All remaining discretes were uniformly distributed amoung the ELMCs and RTs. That is, each device connected to the data bus with the exception of the GCUs contributes equally to the total discrete input and output requirements.

(3) Response Time

In order to compute the processor loading and data bus loading the response time of the system must be known. Response time refers to the maximum time required to detect a change in an event, process the information and then send a response on the data bus. A bimodal response time was used in this study. For the power system, approximately 95% of the discrete data must be input to the power processor, processed and results output within 300 ms. The

remaining 5% of the equations and discrete data must be processed for a 50 ms response time. The 50 ms response time pertains to events which require power bus switching for power distribution reconfiguration.

(4) Avionics Bus Loading

Avionics bus loading is necessary so the bus loading capacity for an integrated power and avionics data bus architecture can be sized. In order to determine realistic bus loading for the avionics suite, the following aircraft missions were studied: fighter, attack, reconnaissance, trainer, electronic warfare, and fighter bomber.

Table 7 shows the major avionics complement that was considered for each aircraft mission. The number given in each box represent a relative complexity index number. The baseline index number for any avionics subsystem is 2. A rating of 1 would indicate a less complicated subsystem, that is a subsystem which would have significantly lower data bus traffic than the baseline subsystem. A rating of 3 signifies a more complicated subsystem. The avionics subsystem complement shown in Table 7 was obtained by reviewing typical avionics suites for the F-16, A-10, F-111A, RF-4C, EA-6B, and EF-111 aircraft.

The complexity index is used for comparison of a particular subsystem among the various missions. Note that the cumulative total of the complexity index of all subsystems for each mission cannot be compared among the missions due to wide variations in bus loading requirements. For instance, the ECM subsystem for an electronics warfare mission may contribute 8000 words/sec of bus traffic alone. This is more than 50% of the total estimated bus traffic for a fighter of approximately 14000 words/sec. Note also in Table 7 that the avionics suites for both the reconnaissance and electronic warfare missions do not contain any weapons delivery capability.

In order to establish a representative avionics baseline bus loading model subsystems with a complexity index of 2 were selected. Data for the weapons delivery function (fire control computer, stores management, fire control radar, and laser set), inertial navigation system (INS), and air data computer

TABLE 7
AVIONICS DATA BUS LOADING COMPLEXITY ANALYSIS

AVIONICS SUBSYSTEM / MISSION	CONTROL AND DISPLAY	FIRE CONTROL COMPUTER	INERTIAL NAV SYSTEM	STORES MANAGE	FIRE CONTROL RADAR	AIR DATA COMPUTER	LASER SET	COMM	ECM	IMAGING
FIGHTER	1	2	2	2	2	2	2	2	2	1
ATTACK	1	2	2	2	2	2	2	2	2	2
RECONNISSANCE	2	-	3	-	-	2	-	1	2	3
TRAINER	3	3	2	2	2	2	2	2	2	1
ELECTRONIC WARFARE	2	-	2	-	-	2	-	2	3	1
FIGHTER BOMBER	2	2	2	2	2	2	2	2	2	2

were all taken from published data for the F-16. In addition, F-16 Control and Display (CAD) data was used as no fighter-bomber CAD data was available at the writing of this report. The baseline CAD subsystem will therefore consist of a fire control and navigation panel, head-up-display (HUD), and radar display. Electronic counter measures (ECM), imaging, and communications data bus loading was based on data developed at Boeing for a multi-role bomber. The ECM subsystem function is assumed to consist of flare and chaff dispersal. The imaging subsystem baseline consists of a forward looking radar.

Perturbations from the baseline in the form of increased complexity for the CAD, INS, ECM, and imaging subsystems for the reconnaisance, trainer, and electronic warfare missions were examined. As shown in Table 7, significant complexity increases in the INS and the imaging subsystem exist for the reconnaissance mission. Reconnaissance missions are assumed to require a very accurate INS and the imaging subsystem would contain side looking radar, infra-red mapping equipment, high resolution cameras, and TV cameras as well as forward looking radar. The increases in data bus loading incurred by these more complicated subsystems is expected to be neutralized by the absence of a weapons delivery capability.

In the case of the trainer, a more complicated CAD subsystem is anticipated due to the requirement for dual control and displays, and an additional monitor function for one of the pilots. The expected increase in bus traffic is estimated to be less than 20% for this subsystem.

The electronics warfare mission represents perhaps the greatest potential for increased data bus traffic from the baseline due to the large amount of data needed to identify threats and jamming as appropriate. Data from the multi-role bomber study indicates that ECM can add 8000 words/sec to bus traffic. Again, this is offset by a lack of weapon delivery capability for this mission. Using the F16 data the weapons delivery capability would add 8975 words/sec to the data bus, more than offsetting the ECM traffic.

Based on the above analysis, the number of words/sec shown in Table 8 were selected as the baseline avionics data bus loading model. The percent bus loading, based on approximately 40,000 data words/sec maximum bus loading for the MIL-STD-1553B data bus, was 36%.

TABLE 8
BASELINE AVIONICS DATA BUS LOADING

SUBSYSTEM	WORDS/SEC
Control and Display	661
Weapons Delivery	8975
Inertial Navigation	3350
Air Data Computer	775
Communications	128
ECM	205
Imaging Radar	128
	14,222

b. Technical Analysis

This section describes the technical analysis performed on the three separate architectures considered for electrical control. These three architectures are shown graphically in Figure 12 and are described below:

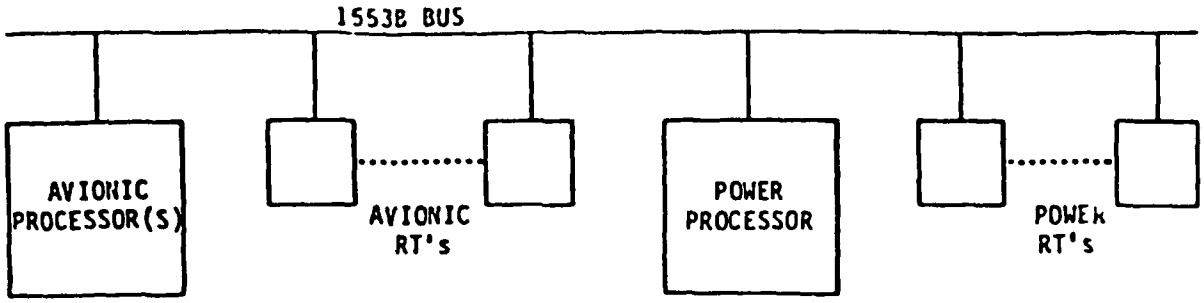
a) Integrated: The electrical control system is on the same bus as the avionics.

b) Hierarchical: The electrical control system is on a separate bus but is connected to the avionic bus through an interbus processor.

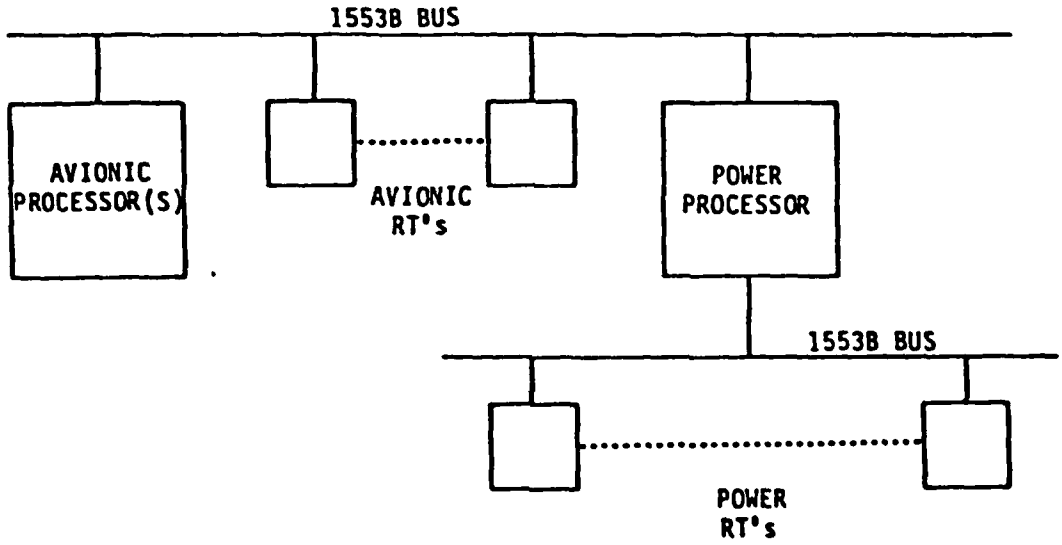
c) Non-Integrated: The electrical control system is not connected to the avionic system by any multiplex data bus.

For each of these architectures the following analyses were performed:

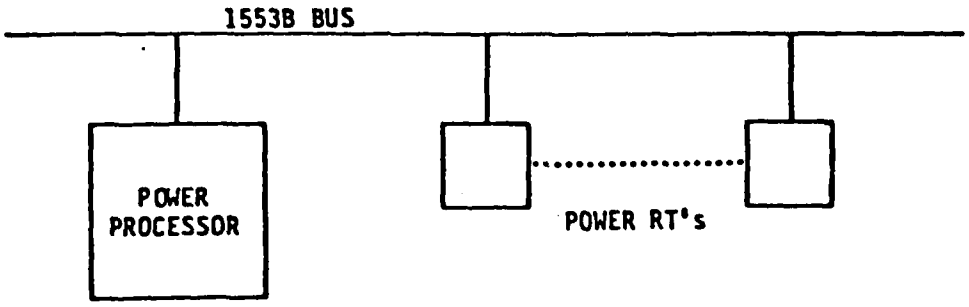
a) Processor loading: This is calculated as the total time required to calculate the necessary set of logic equations in a minor cycle divided by the time in a minor cycle. The accepted limit for processor loading is 50%.



A: INTEGRATED ARCHITECTURE



B: HIERARCHICAL ARCHITECTURE



C: NON-INTEGRATED POWER BUS

Figure 12 Data Bus Architecture Configuration

b) Bus Loading: This is calculated as the time required to transmit the necessary set of data, including overhead, in a minor cycle divided by the time in a minor cycle. The accepted limit for bus loading is 50%.

c) Memory requirements: The total memory requirements for the logic equations and the executive is calculated.

d) Reliability: An architectural reliability for comparison of the integrated and hierarchical concepts is calculated.

e) Number of processors required: an estimate of the total number of processors is given for each architecture.

f) Smart RTs: The effect on processor loading and bus loading is analyzed using distributed processing with smart RTs.

(1) General Assumptions

The analysis of the three data bus architectures were made based on the assumptions listed below. These assumptions apply to all of the three architectures studied.

a) Response time is defined to be the time required for a data change in one RT to be received by the processor, processed, and transmitted to all other RT's that require the data.

b) Bus I/O and processing are bimodal to meet separate response times of 50 msec and 300 msec. The messages that require a 50 msec response time are 5 percent of the total.

c) The system uses a MIL-STD-1553B multiplex data bus.

d) All bus transmissions are terminal-to-controller or controller-to-terminal. These are no terminal-to-terminal transmissions.

e) All bus transmissions are synchronous.

f) The system runs at 128 minor cycles per second. This provides 7.8125 msec in each minor cycle.

g) All remote terminals in the system receive the minor cycle synchronization mode code each minor cycle.

h) All data words transmitted on the bus are packed 12 data bits per 16 bit word. This will allow expansion of 4 bits per word.

i) For each architecture, there is one power system processor. This processor is a MIL-STD-1750 machine with 128 K words (16 bits each) of memory.

j) For each architecture there are ten power RTs. This includes 5 ELMCs. In the smart RT configurations, the 5 ELMCs will have a Z8002 microprocessor as the processing element.

The following assumptions apply only to the integrated data bus architecture.

k) The power system processor is a remote processor on the data bus. The bus controller is the avionics processor.

l) All power applications processing will occur in the power system processor. There will be no power processing in the avionic processor(s).

m) Bus loading for the avionics I/O is 36%.

n) The avionic bus controller processor will send a minor cycle synchronization mode code to the power system processor and to each of the power RTs every minor cycle. The bus time required to do this is included in the avionics bus load.

(2) Processor Loading

Processor loading is defined as the amount of time within a minor cycle that the processor is busy executing application and executive code. The loading of the power system processor, smart RT with Z8002 microprocessor, and executive loading are all discussed.

Processor Loading - Equations Only

The processing time for the electrical system equations was derived by coding representative equations in the JOVIAL J73/I higher order language and then adding the execution times of the assembly language instructions that result when they are compiled (Reference 16). The electrical system equations are organized into three categories as described in section II.2.a(1). The execution time per equation and the number of equations for SSPC complements of 500, 450, 400 and 350, respectively, is shown in Table 9:

TABLE 9

EXECUTION TIME PER EQUATION AND NUMBER OF EQUATIONS VS SSPC COMPLEMENT

		Number of Equations			
Equation Category	Processing time per equation	500 SSPCs	450 SSPCs	400 SSPCs	350 SSPCs
CAT I					
form 1	16.5 usec	208	187	166	146
form 2	49.25 usec	236	212	189	165
form 3	134 usec	45	40	36	31.5
form 4	1519 usec	6	5.4	4.8	4.2
CAT II	38 usec	500	450	400	350
CAT III	34 usec	500	450	400	350

The total execution time for all equations in each of the four SSPC complements is shown in Table 10:

TABLE 10
TOTAL EXECUTION TIME VS SSPC COMPLEMENTS

SSPC Complement	Total Time
500	74735 usec
450	59489 usec
400	52962 usec
350	46336 usec

Processor loading was calculated for both dumb RT and smart RT configurations. In the dumb RT configuration the power system processor calculates all equations. In the smart RT configuration the ELMC RT's calculate the category II and III equations and the processor calculates only the category I equations

Equation calculation is bimodal to meet response time of 50 msec and 300 msec. In a dumb RT configuration, 5% of the calculations are spread over 2 minor cycles to meet the 50 msec response time and 95% of the calculations are spread over 32 minor cycles to meet the 300 msec response time. In a smart RT configuration, 5% of the calculations are spread over 2 minor cycles and 95% of the calculations are spread over 16 minor cycles.

The processor loading for equations only for each of the four SSPC complements is shown in Table 11. These processor loading numbers are valid for all three data bus architectures. The method for calculating the processor loading is shown in Appendix A.

TABLE 11
PROCESSOR LOADING - EQUATIONS ONLY

No of SSPCs	500	450	400	350
Dumb RTs	46%	42%	37%	32%
Smart RTs	35%	29%	26%	23%

RT Loading - Equations Only

In the smart RT configuration, each of the 5 ELMC RTs will have a Z8002 processing element. Only the processing time for the 500 SSPC complement was calculated for the smart RTs. The Category II and III equations are divided equally between the 5 smart RTs. As with power processor loading, the calculation of equations is bimodal to meet response times of 50 and 300 msec. The processing load for each RT is 21% with 5% of the processing spread over 2 minor cycles and 95% of the processing spread over 16 minor cycles.

Processor Loading - Executive

Because each of the three architectures will require a different executive, the processing time required by the executive is different for each architecture.

In the integrated architecture, the executive is responsible only for actions local to the power system processor. It is not responsible for bus control or system actions. In the hierarchical and non-integrated architectures, the power system processor will have an executive that is responsible for both system actions and local actions. In addition the hierarchical power processor executive will have slightly more processing requirements as a result of being a remote on the avionics bus. In relation to one another, the hierarchical executive will require the most overhead, the non-integrated executive is second and the integrated executive will require the least.

The actual percentage of processor loading during a minor cycle required by the executive is dependent on the type of executive as stated above, and on how the applications software is structured and the amount of executive services the application software requires. The more applications tasks there are, the more overhead the executive requires. A general assumption is that the executive overhead for servicing applications tasks is about 20% of the applications processor load. For example: if the processor load for the application tasks only is 35%, then the executive would have an additional processor load of about 20% of 35 or 7%, for a total processor load of 42%. A general assumption for executive services of system actions is about 15% if

the executive is the bus controller and about 7% if the executive is a remote on the bus. If, in the example just mentioned, the power system processor is in a hierarchical configuration, an estimate of the total processor load in one minor cycle is 35% (application) + 7% (local executive service) + 15% (executive services for power bus) + 7% (executive services for avionic bus) = 64%. If the overhead processor loading is added to that for the loading due to equations only then total processor loading is as shown in Table 12.

TABLE 12
TOTAL PROCESSOR LOADING (%)

SSPC Count	Dumb RT			Smart RT (1)		
	Non-Int	Hier (2)	Int	Non-Int	Hier (2)	Int
500	70	77	55	57	64	42
450	65	72	50	50	57	35
400	59	66	44	46	53	31
350	53	60	38	43	50	28

(1) 21% Processor Loading Assigned to ELMC RTs.
(2) Includes Local, Power Bus, and Avionics Bus Executive Services.

(3) Data Bus Loading

Data bus loading is defined as the time required to transmit the required data, including overhead, divided by the total time available. The overhead included in the bus loading analysis is inter-message gap time and message response time.

Bus loading was calculated for dumb and smart RT configurations in each of the three architectures for the four different SSPC complements. The bus traffic for the dumb and smart RT configurations are shown in Tables 13 and 14 respectively.

The number of discrete inputs for RT1, RT2 and RT3 are reduced by 83 in the integrated and hierarchical architectures. These are avionics discretes that are sent to the power processor directly over the avionics system bus

TABLE 13

NUMBER OF DATA BITS TRANSMITTED-DUMB RT CONFIGURATION

Terminal Type	Discrete Inputs SSPC Complement								Discrete Outputs SSPC Complement			
	500		450		400		350		500	450	400	350
	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)				
ELMC1	250	250	225	225	200	200	175	175	118	106	94	83
ELMC2	250	250	225	225	200	200	175	175	118	106	94	83
RT1	167	250	150	225	134	200	117	175	118	106	94	83
GCU1	50	50	45	45	40	40	35	35	50	45	40	35
ELMC3	250	250	225	225	200	200	175	175	118	106	94	83
ELMC4	250	250	225	225	200	200	175	175	118	106	94	83
ELMC5	250	250	225	225	200	200	175	175	118	106	94	83
RT2	167	250	150	225	134	200	117	175	118	106	94	83
GCU2	50	50	45	45	40	40	35	35	50	45	40	35
RT3	167	250	150	225	134	250	117	175	118	106	94	83

(1) Integrated and hierarchical architecture
(2) Non-integrated architecture

TABLE 14

NUMBER OF DATA BITS TRANSMITTED-SMART RT CONFIGURATION

Terminal Type	Discrete Inputs SSPC Complement								Discrete Outputs SSPC Complement			
	500		450		400		350		500	450	400	350
	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)				
ELMC1	150	150	135	135	120	120	105	105	118	106	94	83
ELMC2	150	150	135	135	120	120	105	105	118	106	94	83
RT1	167	250	150	225	134	200	117	175	118	106	94	83
GCU1	50	50	45	45	40	40	35	35	50	45	40	35
ELMC3	150	150	135	135	120	120	105	105	118	106	94	83
ELMC4	150	150	135	135	120	120	105	105	118	106	94	83
ELMC5	150	150	135	135	120	120	105	105	118	106	94	83
RT2	167	250	150	225	134	200	117	175	118	106	94	83
GCU2	50	50	45	45	40	40	35	35	50	45	40	35
RT3	167	250	150	225	134	200	117	175	118	106	94	83

(1) Integrated and hierarchical architecture
(2) Non-integrated architecture

Data bus I/O is bimodal to meet response times of 50 msec and 300 msec. In a dumb RT configuration 5% of the I/O is spread over 2 minor cycles to meet the 50 msec response time and 95% of the I/O is spread over 4 minor cycles to meet the 300 msec response time. In the smart RT configuration, 5% of the I/O is spread over 2 minor cycles and 95% of the I/O is spread over 16 minor cycles.

The bus loading results for each architecture for the four SSPC complements are shown in Table 15. For the integrated architecture, it is assumed that the minor cycle synchronization mode code to each of the power system devices is part of the avionics bus load. The bus loading figures for the hierarchical and non-integrated architectures includes the overhead of sending the minor cycle mode codes to the power devices.

TABLE 15
DATA BUS LOADING

Architecture Type	% Loading Per SSPC Complement			
	500	450	400	350
Integrated				
Dumb RT	64	62	61	59
Smart RT	49	49	49	48
Hierarchical				
Dumb RT	37	36	34	33
Smart RT	22	22	22	21
Non-integrated				
Dumb RT	38	37	35	34
Smart RT	23	23	23	22

(4) Memory Requirements

An estimate of the memory requirements were made for the power system processor and for a smart RT. The elements that are competing for memory are listed as follows:

- o executable code for applications equations
- o other executable code for application
- o application data
- o executive code
- o executive data

The memory requirements for equation calculations can be determined exactly but only estimates can be made for the others. The memory requirements for the equations was determined by coding representative equations in the J73/I higher order language. The compiled result gives the memory required per equation type in Table 16.

TABLE 16
MEMORY REQUIREMENTS

Equation Type	No. of Words AN/AYK-15A	Z8002
CAT I		
Form 1	11	--
Form 2	27	--
Form 3	84	--
Form 4	954	--
CAT II	24	33
CAT III	21	26

Table 17 shows the total memory requirements for equations only for the four SSPC complements. Because the number of equations being executed is independent of the architecture, these figures apply to all three architectures studied.

TABLE 17
TOTAL MEMORY REQUIRED - EQUATIONS ONLY

	No. of Words Per SSPC Complement			
Processor Type	500	450	400	350
AN/AYK-15A Dumb RT	40911	36543	32531	28464
AN/AYK-15A Smart RT	18164	16348	14531	12714
Z8002	5900	5310	4720	4130

Other executable code for applications includes such things as control logic for the equations themselves and applications processing other than equations. The memory required for this is totally dependent on the design and structure of the applications software and cannot be accurately determined here.

Estimates can be made, however, for the memory requirements of the executive and the executive data base. The power system processor in each architecture type will require a different executive size and executive data base size. Estimates on the executive size are: 3000 words for the integrated power processor, 7000 words for the hierarchical processor and 5000 words for the non-integrated power system processor. The executive data base is dependent on the type of executive and the structure of the application software. A large number of application tasks, events, etc. results in a larger executive data base. A conservative estimate on the size of the executive data base for an average set of applications tasks is 5000 words.

(5) Reliability

Reliability comparisions for the three architectures are made using the generalized reliability model in Figure 13. Since the 1553B data bus is dual redundant, connectors are shown having parallel paths. Processors, RTs, and ELMCs are shown as series paths since for our initial analysis it is assumed that these elements do not have redundant data paths. The assumption is made

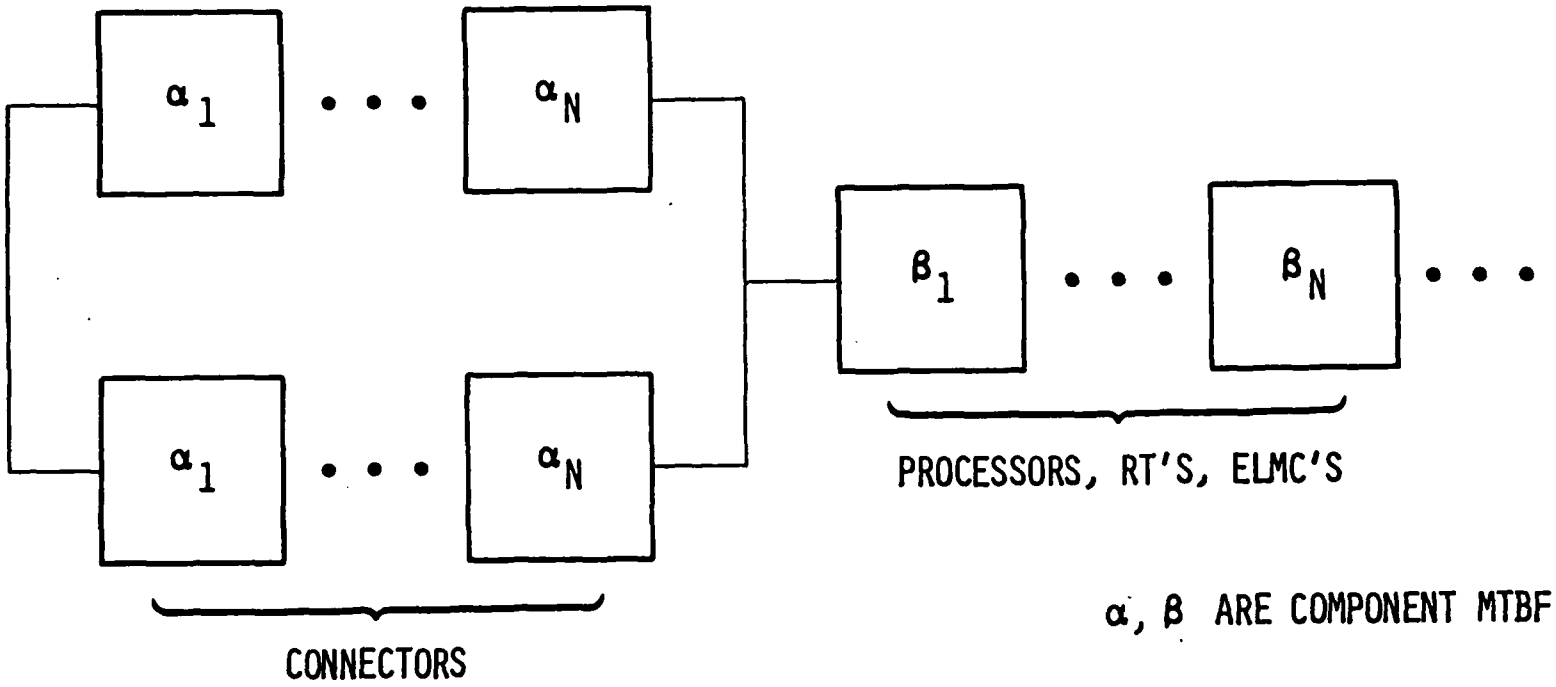


Figure 13 General Reliability Model

in the analysis that all elements have independent MTBF. Also, implicitly assumed in the model is that either one or the other data bus is used to access all RTs and ELMCs.

Reliability computed in this section is not an overall system reliability. It is a computer architecture reliability and its main purpose is for comparison of the three architectural configurations. In Figure 13 α_1 through α_n are the MTBFs for the connectors. β_1 through β_n are the MTFBs for processor, RTs, and ELMCs.

The following assumptions were used in the reliability analysis:

a) 2.5 HR mission time for the tactical two engine airplane.
b) Processor MTBF - 3000 HRS.: This MTBF was obtained from the DAIS AN/AYK-15A specification in Reference 17.
c) GCU MTBF - 4000 HRS: obtained from Reference 4.
d) ELMC MTBF - 1159 HRS
e) RT MTBF - 2354 HRS
f) Connector MTBF = $1.8X10^6$ HRS

Assumptions d-f are based on Harris Corportation hardware experience.

Reliability for a system component is expressed as follows:

$$R = EXP\ (-T/MTBF)$$

where T is the time.

Using the reliability model in Figure 13, the reliability equations for each of the three architectures are as follows:

$$\text{NON INTEGRATED:} \quad R(T) = R_{PP}\ R_{ELMC}^{5}\ R_{RT}^{3}\ R_{GCU}^{2}\ \left[1-(1-R_{CONP})^{2}\right]^{11} \qquad (1)$$

$$\text{HIERARCHICAL:} \quad R(T) = R_{PP}\ R_{AP}\ R_{ELMC}^{5}\ R_{RT}^{10}\ R_{GCU}^{2}\ \left[1-(1-R_{CONP})^{2}\right]^{11}\left[1-(1-R_{CONA})^{2}\right]^{8} \qquad (2)$$

$$\text{INTEGRATED:} \quad R(T) = R_{PP}\ R_{AP}\ R_{ELMC}^{5}\ R_{RT}^{10}\ R_{GCU}^{2}\ \left[1-(1-R_{CONN})^{2}\right]^{19} \qquad (3)$$

Using these equations the reliability for the respective architectures is as follows:

Non-integrated - 0.984
integrated - 0.976
hierarchical - 0.976

Due to the high reliability of the connectors and since an equal number of elements are connected to the data bus for both the hierarchical and integrated architectures, the reliability is the same for these two configurations.

(6) Results of the Technical Analysis

The major conclusion of the technical analysis performed on the three architectures are:

a) Processor loading: smart ELMCs and an integrated architecture are necessary to meet the processing requirements for a two engine tactical aircraft

b) Bus loading: All architectural concepts can meet the two engine tactical aircraft power system control requirements if smart ELMCs are used.

c) Memory: smart ELMCs will require 17% more memory than the dumb ELMC configuration to meet the equation processing requirements.

d) Reliability: the hierarchical and integrated architectures have identical reliability due to the high reliability of connectors.

c. Economic Analysis

Both software and hardware costs of a two engine tactical aircraft electrical power control system architecture were examined. Software costs are for application software development only. These costs are independent of the architecture chosen. Hardware costs are relative to the baseline non-integrated architecture. Only relative hardware costs were obtained since absolute costs from the manufacturers could not be obtained for the hardware at this early stage of development. The effects of SSPC count and architectural differences in costs are also discussed.

(1) Software Development Costs

The development cost of software for a two engine tactical aircraft electrical power control system is dependent on the level of documentation and the number of reviews required. We can assume that for an Air Force contract the full spectrum of documentation and design reviews will be required. Software development cost at this level of effort will be $90,000 per 1000 words of code. This cost figure is based on Boeing's experience during the development of the executive software for the Single Processor Synchronous Executive (SPSE) under AFAL contract F33615-77-C-1252.

The executive software to be used will be the DAIS executive or a derivative of the DAIS executive. It can be assumed then that the executive software will be free of development costs. The application software for the power system appears to be fairly repetitious (many equations of the same type). This factor has the potential of lowering the software cost.

In a smart RT configuration software for the RT processor will have to be written in addition to the main power system processor. However, the impact of this should be minimal if J73 HOL can be used as the source language for

both machines. Using the application software memory requirements defined previously and the above cost factors, the application software development costs as follows:

SSPC COUNT	DUMB ELMC ($K)	SMART ELMC ($K)
500	3681	4293
450	3285	3852
400	2925	3229
350	2565	3006

(2) Hardware Costs

Hardware costs of the hierarchical and integrated architectures relative to the baseline non-integrated approach were determined. These relative hardware costs reflect differences in memory, ELMC configuration (dumb versus smart), RT and processing requirements only.

The cost analysis was done using the following hardware input cost data supplied by the Harris Corporation Melbourne, Fl.

a) Memory: 8,000 16 bit word module - $500/module

b) SSPCs: 2 to 4 SSPCs per module - $1000/module

c) Discrete signal interface module: 64 inputs, 32 outputs - $500/module

d) Additional costs needed to make "Dumb" ELMC "Smart" - $3750/ELMC

In addition to the above inputs, the additional cost of a dual avionics and power bus interface for the hierarchical architecture would be $5000. This cost was provided by the Sperry Corporation.

Using the above inputs, the relative costs of the integrated and hierarchical architectures compared to the non-integrated architecture are as follows:

Architecture	Relative Hardware Costs
Integrated	
249 less discretes	-1.5K
Hierarchical	
249 less discretes	-1.5K
two data bus interfaces	5.0K
	+3.5K

The relative hardware and cost reduction as a function of SSPC count for the baseline architecture is as follows:

SSPC Count	Relative # of SSPC Modules	Relative # of Discrete Modules	Relative Costs Reduction ($K)
500	0	0	0
450	-2	0	-10
400	-5	0	-25
350	-7	-2	-38*

* For hierarchical and integrated architecture ($-36.5K)

The reduction in relative hardware cost is $1.5K for the integrated and hierarchical architectures because these architectures have 249 discretes less than the baseline architecture so a 30% reduction in SSPC count (350) results in the saving of one discrete module only.

(3) Relative System Cost Comparison

All architectural configurations studied have identical numbers of ELMCs, RTs, and GCUs. The major differences between the three concepts is in the processor requirements.

The requirements for the power system processor for the non-integrated architecture approach can be met by the DAIS AN/AYK-15A machine both in terms of hardware and software. The requirements for the power system processor for the integrated architecture approach can also be met by the DAIS AN/AYK-15A except that the executive software will not be as extensive since here the

avionics processor will have most of this responsibility. Thus, the software requirements for the integrated architecture processor will be 20% lower than that of the non-integrated architecture processor. This results in a cost reduction for the integrated architecture system over the non-integrated architecture system.

For the hierarchical architecture additional hardware and software will be required to provide the AN/AYK-15A processor with the capability to interface with two data buses and perform the interbus communications in addition to the power system processor functions. The interbus communication will result in a 40% increase in processor executive software requirements. This will, therefore, increase the cost of the hierarchical architecture processor hardware and software over the non-integrated architecture processor. Therefore, the hierarchical architecture system will cost more than the non-integrated architecture system. From an economic standpoint the integrated data bus architecture concept is considered most appropriate for a two engine tactical aircraft.

SECTION III
CONCEPTUAL DESIGN

Three power control system data bus architectures were configured using DAIS concepts to the maximum extent possible. In order to examine the feasibility of integrating the power system control function into the DAIS architecture, two conceptual designs were configured which have varying degrees of integration with the avionics data bus. In the first design, the integrated concept, both avionics and power system control is accomplished using a common data bus. In the second design, the hierarchical concept, a separate data bus is used for the avionics and the power system control. The power system processor is connected to both the avionics and power data buses and performs the additional function of interbus processing.

The third design is the dedicated or non-integrated power system control concept. In this arrangement, the avionics and power system control functions are totally separate with a separate data bus for each. Such an architecture probably could not be justified for a light tactical fighter. However, this concept was used as a baseline for comparing the two approaches described in the paragraph above and for determining the power system control requirements for a light tactical aircraft.

1. DATA BUS ARCHITECTURES

All the data bus architectures presented in this section are based on the DAIS configuration shown in Figure 14. The DAIS architecture consists of federated processors communicating with each other and the other system elements (sensors, weapons, and controls and displays) through a standarized multiplex data bus. Centralized system single-point control is performed by a processor resident software executive that can be relocated for redundancy. Application software is structured to provide modularity, reliability, and transferability. This system architecture is flexible to accommodate a wide variety of avionics configurations, missions, and sensors, which provides redundancy to improve availability, and accommodate changes in technology.

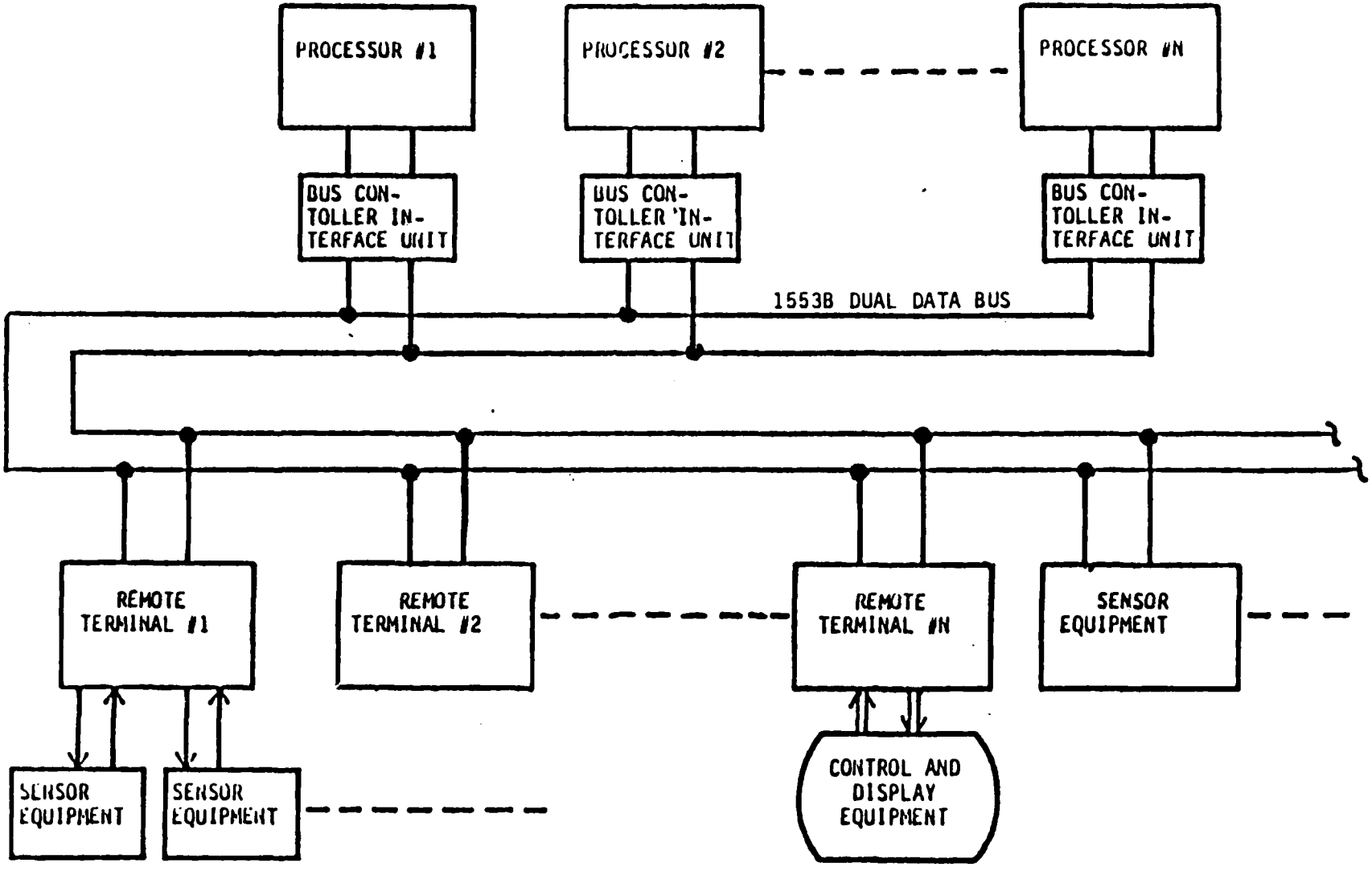


Figure 14 DAIS Data Bus Architecture

The basic architecture is designed for a broad class of configurations where the number of processors can be reduced or enlarged depending upon the avionics and mission requirements. Standardization, modularity, and application independent executive software allows adaptability of this architecture to a broad class of different applications as well as to making mission-to-mission changes in a particular aircraft.

Sensors, weapons, and other subsystems are selected as required for the particular mission and connected to the interface modules of the remote terminals of the multiplex system or connected directly to the multiplex bus.

a. Non-Integrated Data Bus Architecture

The baseline non-integrated data bus architecture is shown in Figure 15. The configuration has two GCUs, 3 RTs, 5 ELMCs and one DAIS type processor. Power management and control software resides in this processor. In the case of a smart ELMC, some of this software is moved to the ELMCs.

The major advantages of this architecture as compared to the other two candidates are:

a) simple system integration and test - due to the separation of avionics and power control functions.

b) easily expandable with minimum software impact - due to similarity with DAIS concept and existing software and hardware modularity.

c) minor changes to existing DAIS software - existing software for DAIS would be "off the shelf" and only an application software package needs to be written.

The major disadvantages of the non-integrated architecture are:

a) redundant avionics RT interfaces - because both buses are physically separate, avionics signals needed in power system management would have to have duplicate interfaces on each data bus.

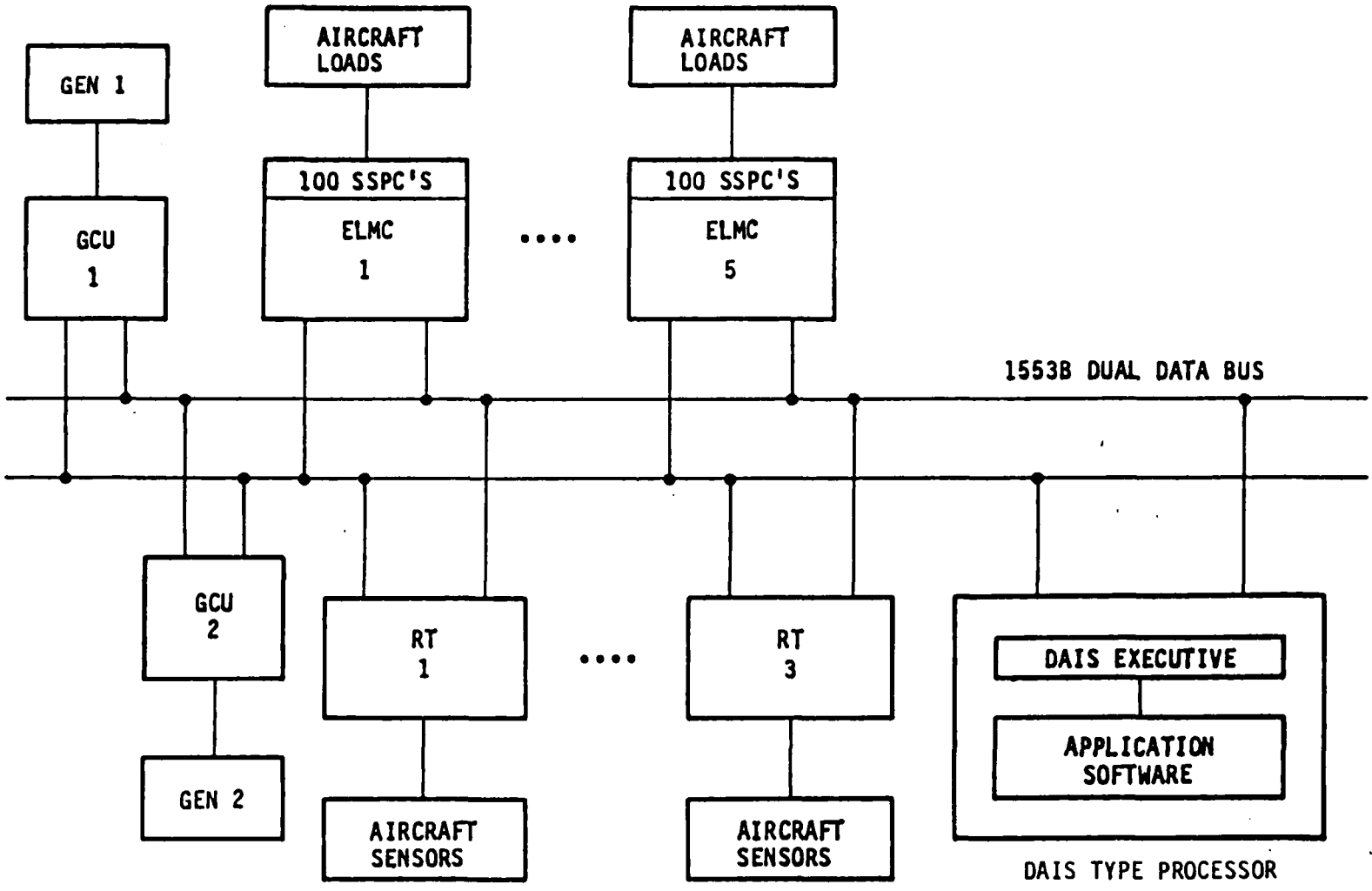


Figure 15 Baseline Non-integrated Architecture

b) additional controls and displays - since there is no data path between the avionics and power control systems, multi-function controls and displays already developed for the DAIS concept could not be utilized.

c) higher bus loading - because avionics signals from the avionics bus cannot be used, these must be obtained by duplicate interfaces.

d) additional weight - due to redundant DAIS components like the controls and displays and bus interface hardware.

b. Integrated Data Bus Architecture

The integrated data bus architecture combines the avionics and power system processors on a single data bus. This concept is shown in Figure 16. The avionics processor acts as the bus controller for the entire data bus and is otherwise dedicated to avionics functions. The power system processor shares the same 1553B data bus and manages and controls its 5 ELMCs, 3 RTs and 2 GCUs. Controls and displays are shared both by the power and avionics system. The major advantages of this concept are:

a) minor changes to existing DAIS concept - in this configuration the power system processor acts as an RT and all executive software would be "off the shelf". Only a power system application software package needs to be designed.

b) least power and weight - when compared to the other two concepts, the integrated approach minimizes the redundant use of DAIS software and hardware.

c) less memory requirements - due to the fact that the power system processor is a RT on the avionics data bus, a full executive is not necessary.

The major disadvantages to the integrated concept are:

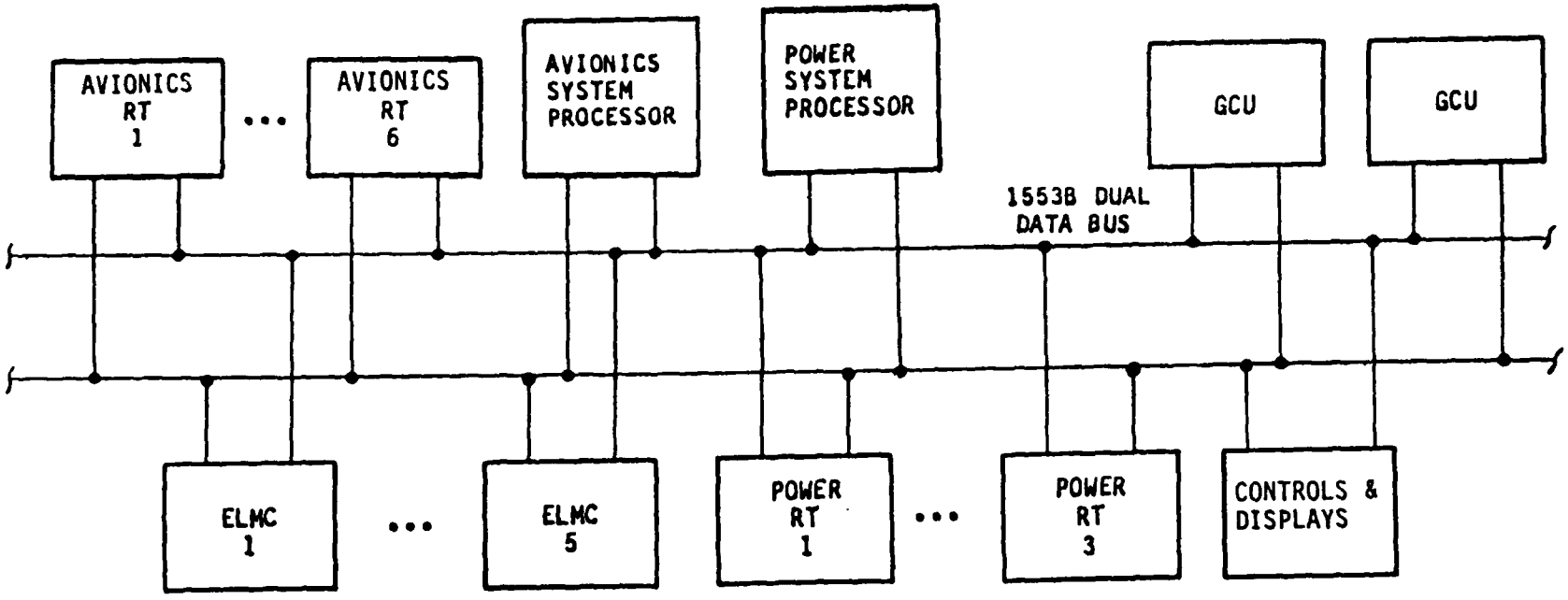


Figure 16 Integrated Architecture

a) interaction of the power and avionics systems - changes to either system can effect the other as the bus traffic has a fixed limit of 1 Megabits per second. Also response time requirements for both systems must be considered in designing data bus protocol and message handling.

b) less expandability - a single DAIS type data bus can be expanded to accomodate up to 32 elements maximum.

c. Hierarchical Data Bus Architecture

The hierarchical concept is shown in Figure 17. The key difference between this arrangement and the previous two concepts is that the power system processor is connected between a separate avionics data bus and power system data bus. The power system processor is a remote terminal on the avionics bus but a bus controller on the power system data bus. The number of RTs, ELMCs, and GCUs needed in order to accomodate the power system control requirements is the same as in previously discussed architectures. The key advantages of this approach are:

a) less bus loading - because avionics data can be obtained from a separate bus, the traffic on the power data bus is reduced.

b) greater expandability - the hierarchical data bus architecture offers almost unlimited growth potential due to the ability to cascade any number of data buses each communicating with the next via an interbus processor.

c) independence of avionics and power system - software development can progress more independently for the avionics and power system since the need to coordinate response time requirements is almost entirely eliminated.

The major disadvantages of this concept are:

a) immature software/hardware: both the interbus processor and its executive software for interfacing to two data buses is still in development.

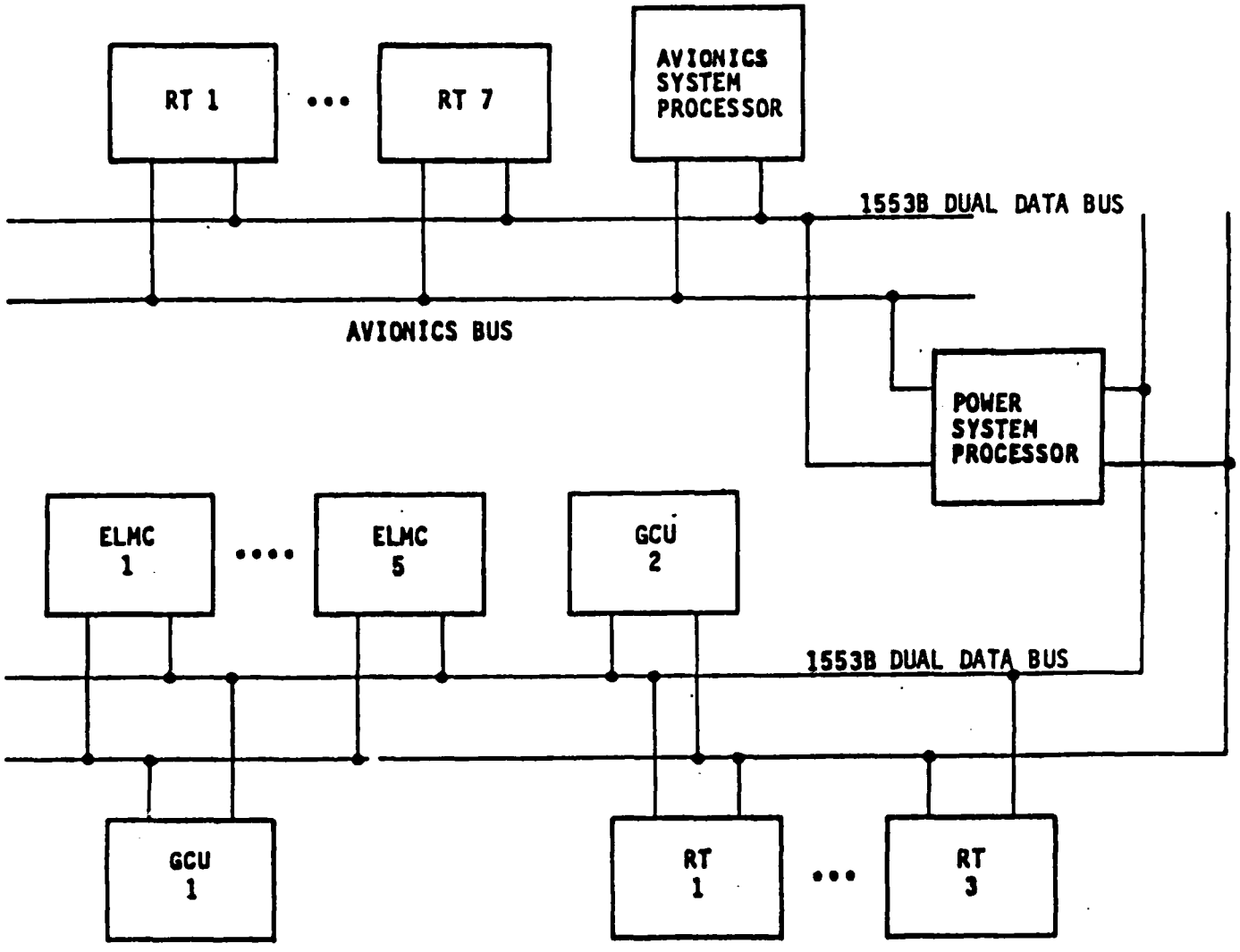


Figure 17 Hierarchical Architecture

b) added weight - more bus interface circuitry and power supplies will be necessary for multiple 1553B data buses than in an integrated approach.

c) higher executive overhead - a single power system processor configured to be both an RT on the avionics bus and the bus controller on the power system data bus incurs enormous software overhead. Processor loading data is described in section II.2.b(2).

d. Redundancy

The goal of redundancy is to eliminate the possibility of the entire system failing because of the failure of any single device. The backup system may not be as powerful as the original system, but at least it will continue to perform in a degraded mode.

For the electrical control system architectures, a study of the redundancy requirements are being conducted beginning with the lowest cost options. At this stage of the electrical system development, there is no need to duplicate everything, and besides there is a shortage of room in a fighter. Redundancy considerations for the power system processor, ELMCs, RTs and GCUs are discussed below.

(1) Power System Processor Redundancy Considerations

In an integrated architecture, when the avionics processor (the bus controller) fails, we will assume that the avionics system will include a backup bus controller (BBC), and that the BBC function will not have to be performed by the power system processor. Since the power system processor is not the bus controller in the integrated architecture, if it fails, there is no need for its backup to be capable of bus control. In the other two architectures, however, the backup to the power system processor must be capable of bus control.

In a hierarchical architecture, the backup to the power system processor need not be an interbus device. It is probably cheaper to have the power RTs have redundant interfaces to the critical avionics sensors to be used in backup mode, in other words, degrade to special purpose non-integrated architecture.

In any of the 3 architectures, the backup to the power system processor can be one of the existing devices on the bus, such as the ELMC or RT. Since the ELMCs will probably already have "smarts", one of them would be a logical choice. The backup related software in the device need not assume the entire processing load of the failed power system processor, but rather, it can make available for transmission to the other power devices a "canned" set of processing results capable of handling a degraded backup mode.

(2) ELMC Redundancy Consideration

It is not cost effective to duplicate each ELMC and its many interfaces. The interfaces to the ELMCs should be designed such that the failure of any one ELMC does not prohibit the power control of critical aircraft systems. In other words, a critical aircraft system is interfaced to more than one ELMC. There will still be the same number of ELMCs in the system.

(3) RT Redundancy Considerations

As with the ELMCs the most important design consideration is that mission critical sensors or displays be interfaced to more than one RT so that the failure of a RT does not deprive the system of critical information. Critical subsystems need a duplicate interface.

(4) GCU Redundancy Considerations

For each generator, there is one generator control unit (GCU). Redundancy for the GCU is derived from the dual generating system (two generators and two GCUs). Although connected to the data bus, the generator control and protection functions operate independent of the data bus. This isolates the generator system from a data bus system failure.

2. POWER SYSTEM PROCESSOR

Per the ground rules of maximum commonality with DAIS, the baseline power System processor will be the AN/AYK-15A DAIS processor per SA421205, MIL-STD-1750 and MIL-STD-1553B. This processor includes the bus controller interface unit (BCIU) and the following features:

- Processor
  - 16 general registers
  - Extensive instruction repertoire (MIL-STD-1750)
  - 379K operation per second throughput based upon specified benchmark program
  - Floating point capability
  - Direct, indirect, immediate, base relative, IC relative, and index addressing modes
  - Programmable interval time
  - Vectored interrupts

- Memory
  - Expandable to 64K words (16 bit words), in 16K word memory mdoules
  - Memory parity and write protect features

- Input and Output
  - Discretes
  - Program controlled
  - Direct memory access
  - External interrupts
  - Multiplex data bus (MIL-STD-1553B)
  - Bus controller
  - Bus active monitor

For the non-integrated, hierarchical, and integrated data bus architectures the above processor will be used with an additional 64K words of memory. In the case of the hierarchical data bus architecture power system processor additional hardware and software to provide the capability to interface with both the avionics data bus and electrical power system data bus will be necessary. This software and hardware is currently in development.

3. REMOTE TERMINAL

Two types of RTs (Smart and Dumb) were examined during the technical analysis to determine their impact on the processor and data bus loading. From the

results of this analysis it was concluded that smart terminals would be required for both the integrated and hierarchical data bus architecture systems. Therefore, no further consideration will be given to development of a dumb RT.

The RT shall be capable of data exchange with and under control of the power system processor via the Standard 1553B Data Bus. The RT shall recognize its address and respond to command words from the power system processor with properly formatted status, data, built-in-test (BIT) results and other requested subsystem information. Control of the RT, its I/O, subsystems and bus interface shall be handled by an imbedded Z8002 microprocessor. This processor shall provide the intelligence to the RT for processing and controlling the discrete and analog inputs and outputs. The analog inputs shall be capable of being either 32 differential (low level) or 64 single ended inputs (high level).

Figure 18 depicts the hardware block diagram of the "Smart" RT. The RT shall contain its own power supply, electronics and I/O circuits to properly perform its task. The following paragraphs define in more detail the functions of each of the blocks shown in Figure 18.

a. Smart RT Processor

The Processor shall contain the Central Processing Unit (CPU), support logic and memories required to perform the various computational tasks of the RT. This shall include but not be limited to:

a) Equation Solving
b) Bus Interface Control
c) I/O Control
d) BIT
e) Status Reporting

The Processor shall receive data from the Bus Interface Unit (BIU), the input interface circuits and BIT. It shall output data to the BIU, the output interface circuits and BIT. None of the I/O interface circuits shall

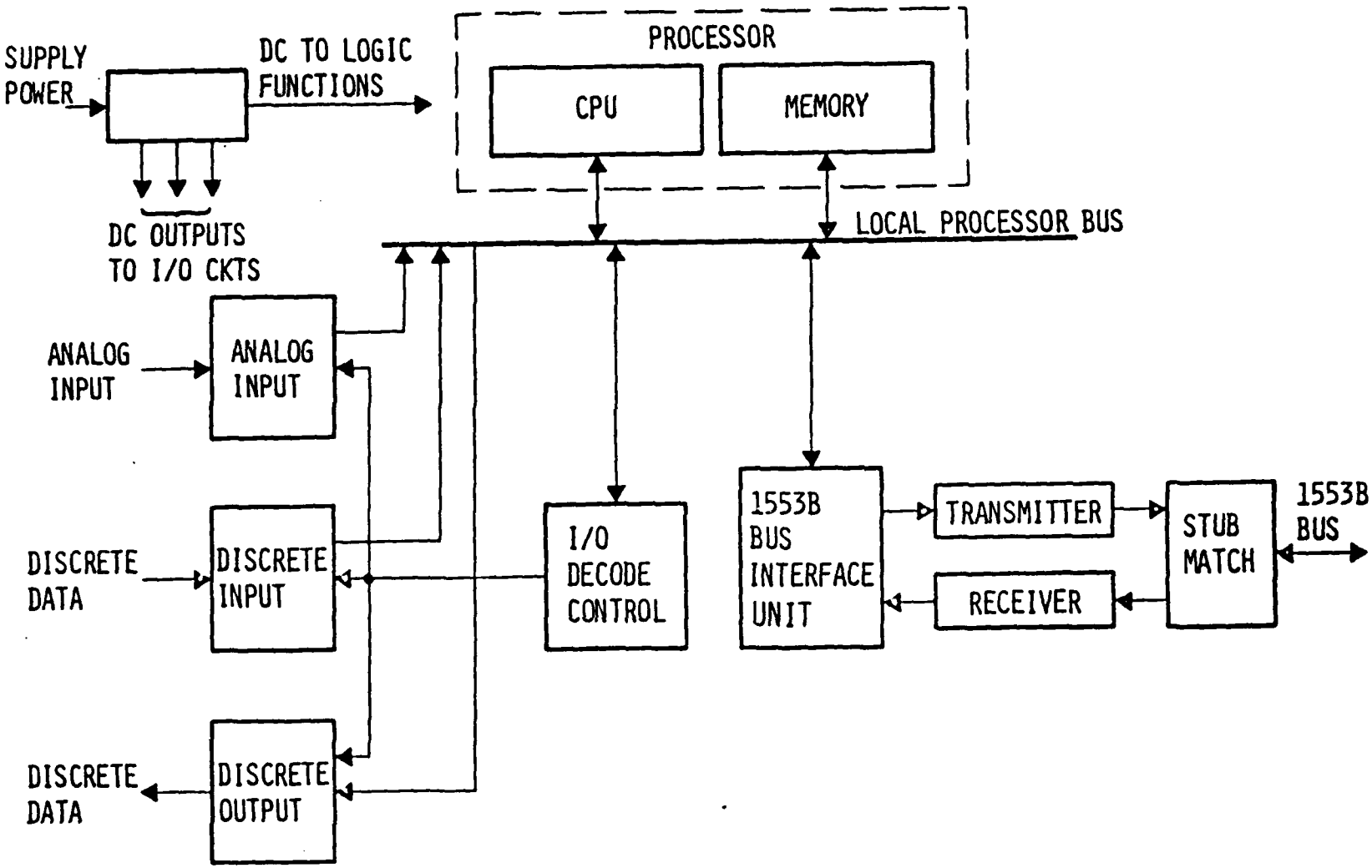


Figure 18 Smart RT Block Diagram

interface directly with the BIU. All routing of data to/from the BIU and to/from the I/O shall be done by and under control of the Processor. The Processor and its supporting software shall be designed to support a frame rate of TBD frames per second. The frame rate shall be such that normal bus interface, equation processing and application functions can be performed with the spare capability of executing lower priority functions on a sequential successive frame basis.

The CPU shall be a Z8002 or similar general purpose microprocessor having the following capabilities:

a) 16 bit word size
b) Arithmetic operations (basic)
c) 16 general purpose registers
d) Direct addressing to 64K bytes
e) Single supply voltage
f) Sophisticated interrupt structure

The Processor memory shall contain both PROM and RAM of sufficient size to support the functions and operations of the RT. The PROM card shall be configured such that it can be addressed as 64K bytes by 8 bits or as 32K bytes by 16 bits. The RAM card shall be configured such that it can be addressed as 16K bytes by 8 bits or as 8K bytes by 16 bits. Both memory types shall have an access time sufficient to support the Processor without creating "wait" states.

b. Bus Interface Unit

The Bus Interface Unit (BIU) has been designed to interface the RT with the 1553B data bus and support the bus protocol as defined in MIL-STD-1553B. The BIU contains the logic to perform its function and a transmitter/receiver section. As a remote, the BIU must first be programmed by the power system processor via the 1553B data bus to perform the following:

a) Output data
   1) Location
   2) Amount
b) Input data
   1) Location
   2) Amount

Once the remote BIU has been programmed, it monitors all traffic on the bus waiting for its specific address. Once its address is decoded, the BIU responds to the particular command being sent. The BIU is also checking the incoming data for parity, bit count, word count and protocol errors. The response word is acted upon by the BIU to insert the proper message sync, parity bits and status information. Once the remote BIU has been initialized, it can execute an entire bus frame without processor intervention when commanded.

The transmitter/receiver portion of the BIU converts the digital data to manchester data for transmission on the bus and manchester data to digital data when receiving data from the bus. A separate unit from the RT, but part of the whole bus interface, is the Data Bus Coupler (DBC). This is a transformer coupled device which isolates the RT from the main bus and provides the proper matching impedances between the RT and the data bus. With the DBC several RT units can be tied to the main bus without interfering with each other.

c. I/O Decode and Control

The I/O Decode and Control shall provide those functions which are repetitive and should be moved from Processor operation. This circuitry shall be closely coupled with Processor activity and shall be used as the main controlling function for the routing of data to and from the different I/O circuits.

d. *Discrete Inputs*

The Discrete Input circuits shall be capable of handling 250 inputs. These circuits shall provide the signal conditioning required and supply the conditioned digitized data to the Processor under control of the I/O Decode and Control section.

e. Discrete Outputs

The Discrete Output circuits shall be capable of handling 118 outputs. These circuits shall provide the drive and signal characteristics required by the driven devices and shall receive their data from the Processor under control of the I/O Decode and Control section.

f. Analog Inputs

The analog input circuitry shall be capable of receiving 32 low level differential inputs or 64 high level single ended inputs. This circuitry shall contain the electronics required to perform the signal conditioning, mode selection, multiplexing and A/D conversion. The data received and converted shall be routed to the Processor under control of the I/O Decode and Control section.

g. Power Supply

The Power Supply shall be a highly efficient supply which receives power from the aircraft power bus and converts it to the regulated voltages required by the RT. The Power Supply shall also contain the circuitry to inform the Processor of a power shutdown or fault to allow graceful shutdown and shall also generate a power-up on reset.

4. ELECTRICAL LOAD MANAGEMENT CENTER

The ELMC (Figure 19) provides the control and management of the electrical power distributed to the loads connected to it. This unit contains a RT embedded in it. It also contains up to 100 SSPCs. The ELMC shall be capable of receiving control inputs, outputting status and controlling the SSPCs. Each SSPC will require one input signal from the RT for on/off control and will send back 2 signals (trip and status) back to the RT. Therefore, of the 118 discrete outputs of the RT, 100 will be assigned to control the SSPCs. Similarly, of the 250 discrete inputs, 200 will be assigned to receive the trip and status of the SSPCs. The balance of the discrete inputs and outputs are utilized for subsystem information handling. The ELMC will be packaged in a full ATR box.

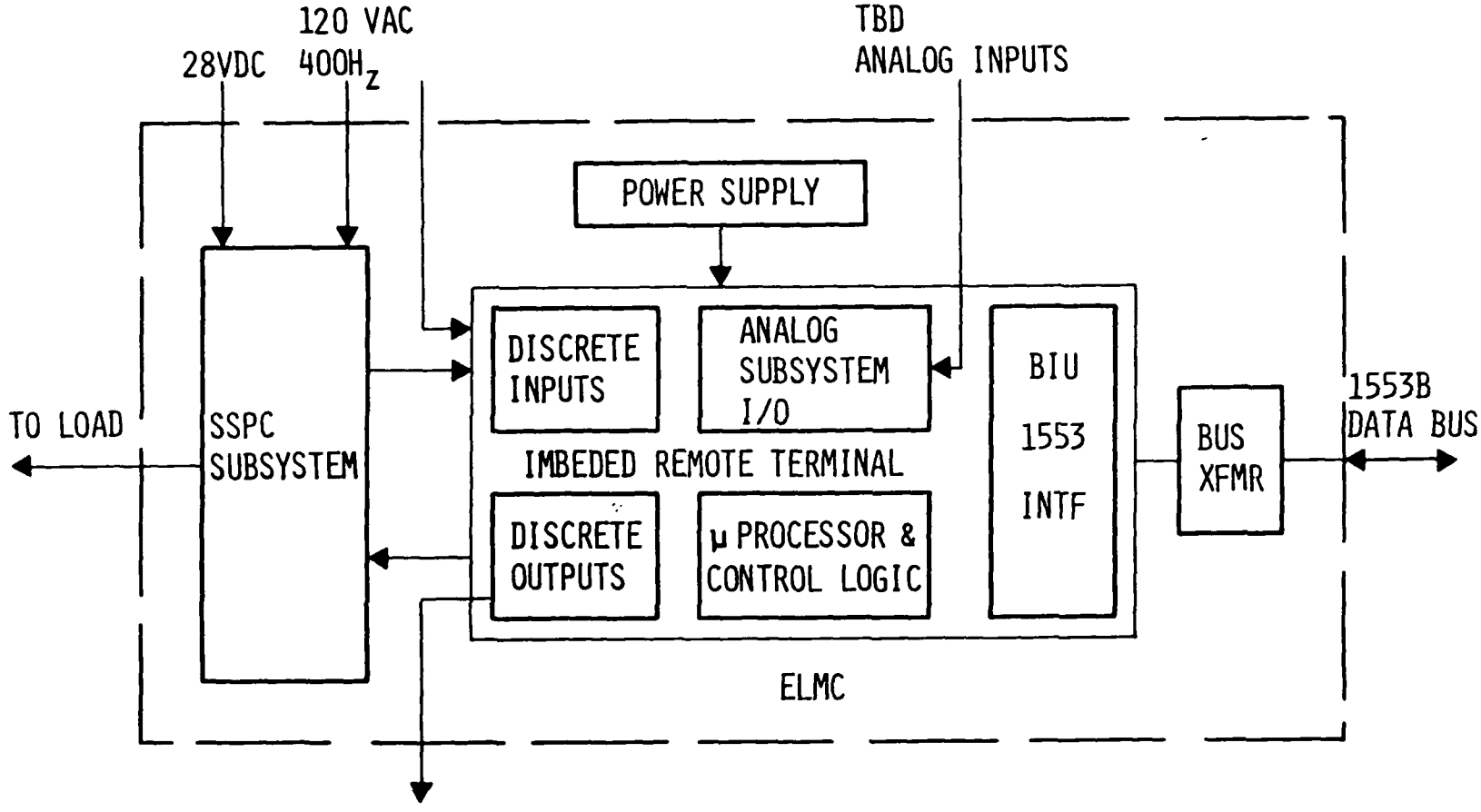


Figure 19 ELMC Block Diagram

5. GENERATOR CONTROL UNIT

The system design is based on having the generator control unit (GCU) "on" the data bus. The GCU is implemented with a microprocessor. The benefit of this implementation is the ease with which information can be transmitted into and out of the GCU by means of the multiplex data bus system.

A block diagram of the GCU is shown in Figure 20. The unit is divided into two sections, the data bus interface module and the generator control module. Although the generator control module is connected to the data bus through the data bus inteface module, the generator control and protection functions operate independent of any bus service functions. This isolates the generator system from the data bus or interface module failure.

6. CONTROLS AND DISPLAYS

An analysis was done to establish the requirements for the controls and displays of the electrical system. The aim of the design is to minimize the controls and only display that information which is essential to the pilot to maintain aircraft safety and to assure mission success.

In keeping with this objective, no panel indicators are to be provided for individual SSPC status or trip indication and individual SSPC reset control. Indication of a failed or tripped SSPC appears on the appropriate subsystem warning panel or equipment warning panel.

A control panel, shown in Figure 21, is required for the DAIS processors. It provides power to the appropriate processor (shown for a 4 processor system) during startup and restart control for any architecture.

CRT displays dedicated to the electrical system is not feasible in a two engine tactical aircraft; however, it is feasible to display electrical system data on the avionics display units. This integrated CRT display concept is possible with the integrated data bus architecture and the hierarchical data bus architecture. An example of this integrated controls/displays concept, which uses existing DAIS hardware, is shown in Figure 22. Only key system failures which affect the mission success will be displayed on the CRT.

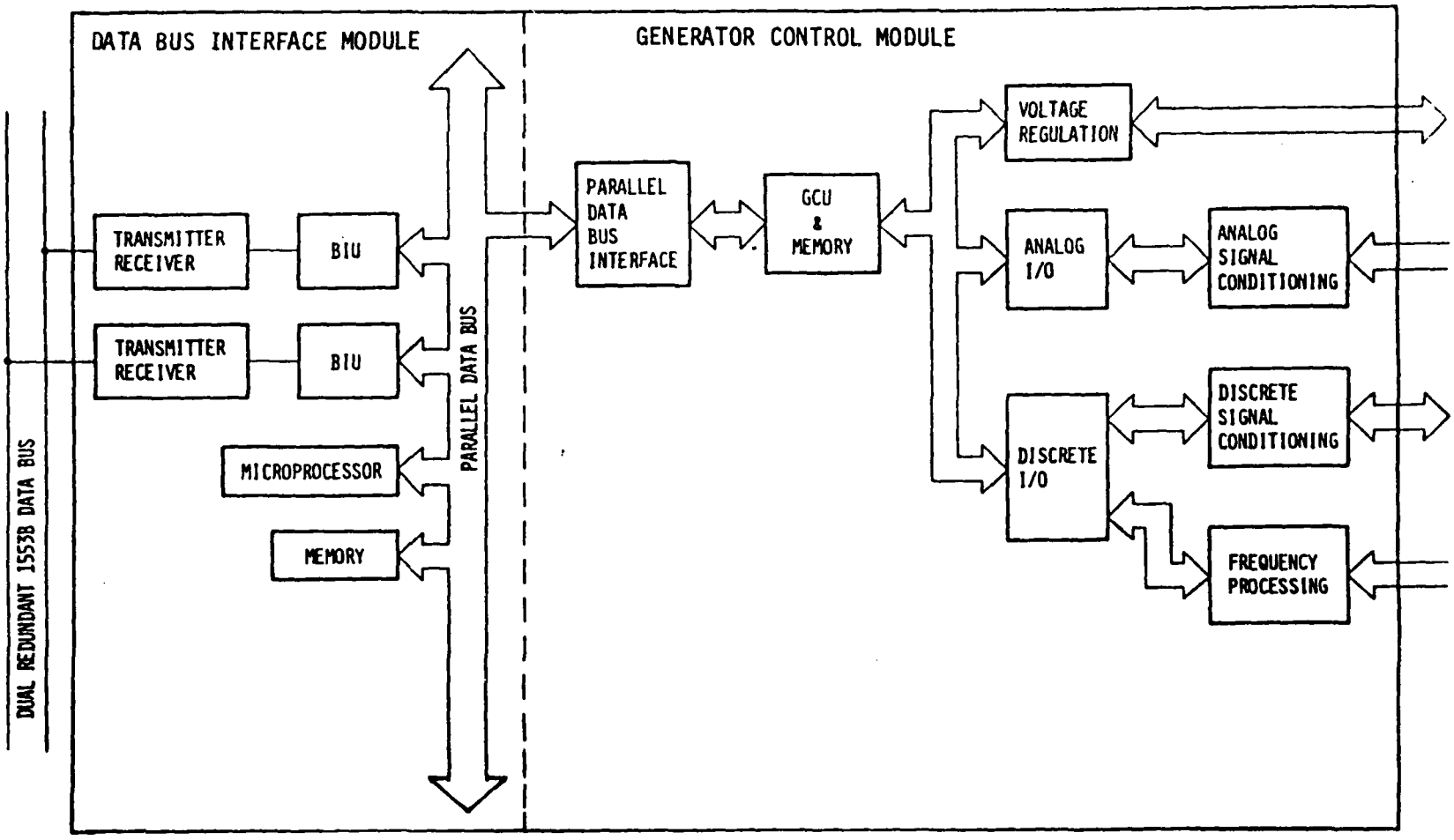


Figure 20 GCU Block Diagram

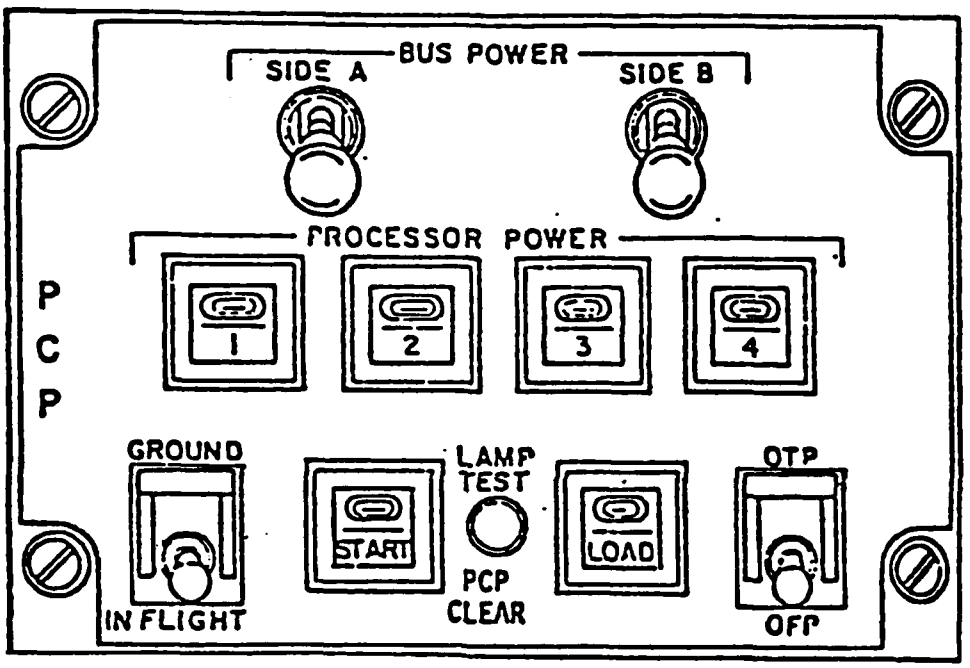


Figure 21 DAIS Processor Control Panel

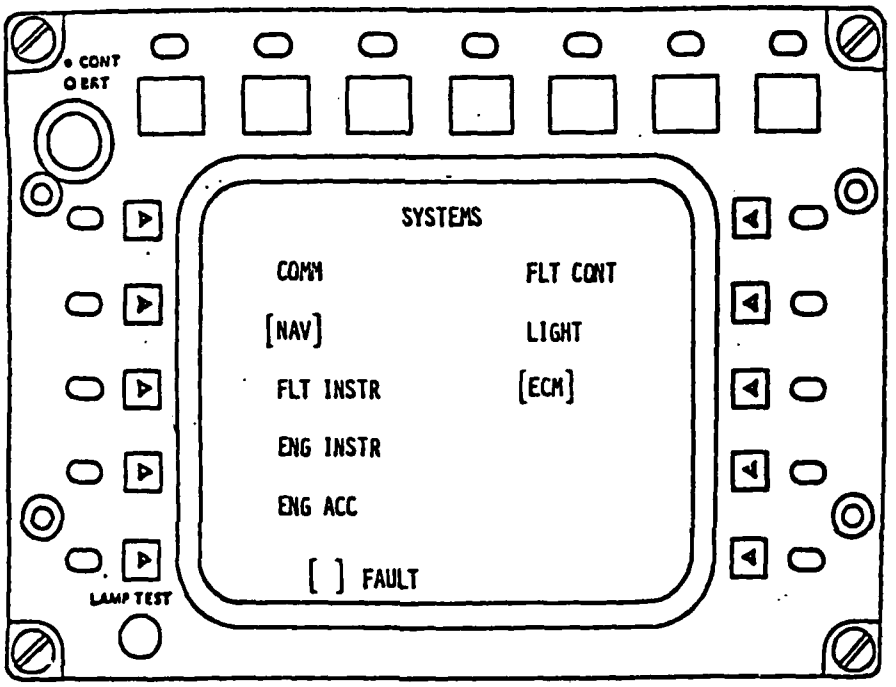


Figure 22 DAIS Integrated Controls/Displays

SECTION IV
POWER SYSTEM SIMULATOR

The Aero Propulsion Laboratory facilities were assessed for application to the AEPS laboratory simulator. A floor plan of the laboratory is shown in Figure 23. The control room has a controlled environment which is suitable to house laboratory and computer equipment; however, there is no room for additional equipment. A floor plan of the control room is shown in Figure 24.

The support equipment for the AEPS laboratory simulator will require a controlled environment. Although the aircraft electrical system portion of the simulator will not need this type of environment, it is desirable to have the aircraft equipment and the support equipment in the same room. A new controlled environment room is needed which will house the laboratory simulator. This room should be located near the generator drive room and the control room. A proposed location for this simulator room is shown in Figure 23.

Since the objective of the laboratory simulator is to demonstrate and evaluate the technology and not to simulate actual aircraft installation, a simulator design which allows easy access to the equipment and allows easy system reconfiguration is desirable. A concept using modular elements mounted on panels is suggested.

For optimum utilization of laboratory space, a wall mounted simulator, as shown in Figure 25, is recommended. The wall mounted simulator will have racks for mounting the electrical system and simulator boxes. The simulator structure, although wall mounted for greatest support, will be spaced approximately five feet from the wall for access to make layout changes and for cooling of the electronic equipment.

A block diagram of a proposed simulator system is shown in Figure 26. This simulator system will support the integrated, hierarchical, and non-integrated architectures. Two computers are used to simulate the avionics system, an avionics simulation computer and a RT simulation computer. The bus monitor

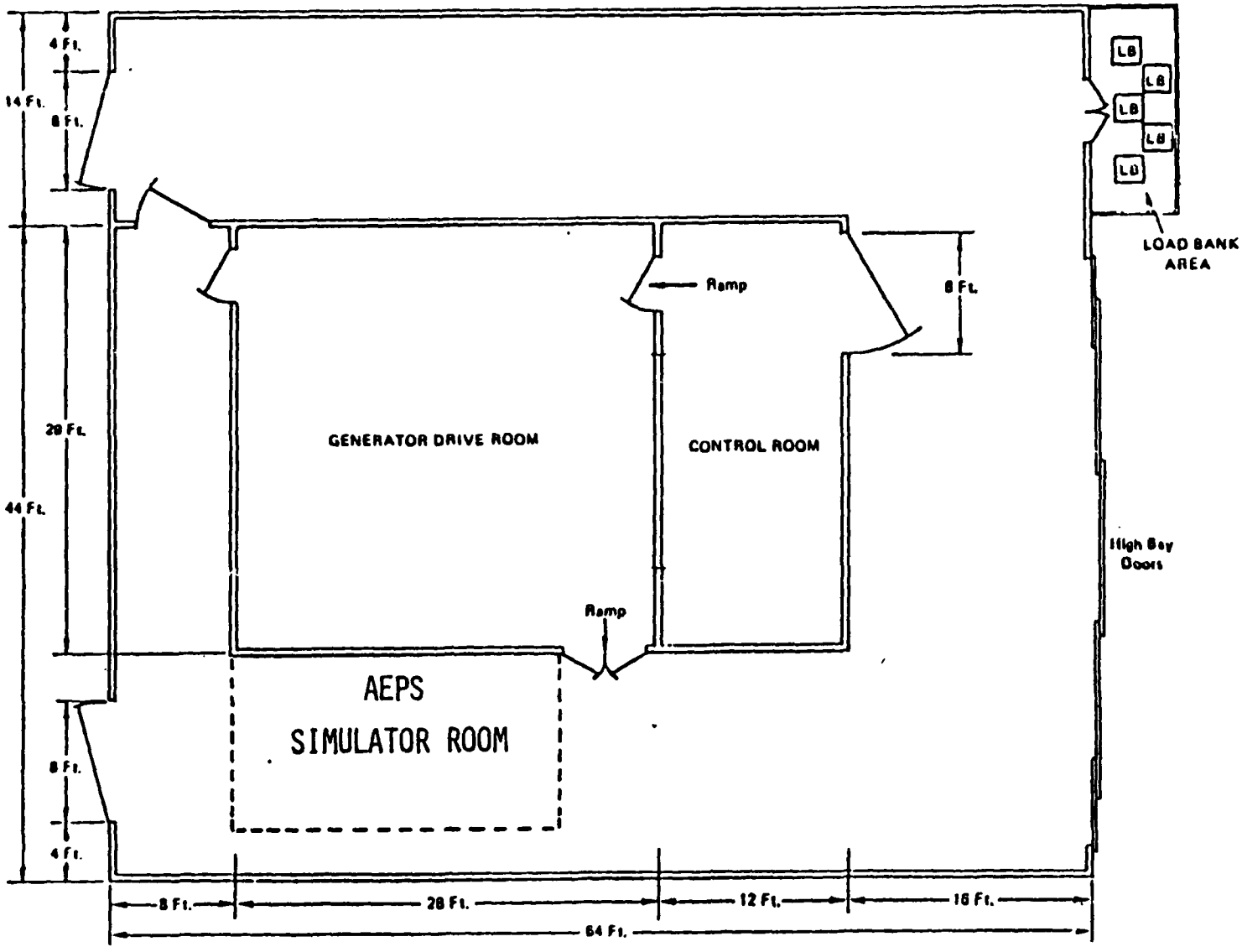


Figure 23 APL Laboratory Floor Plan

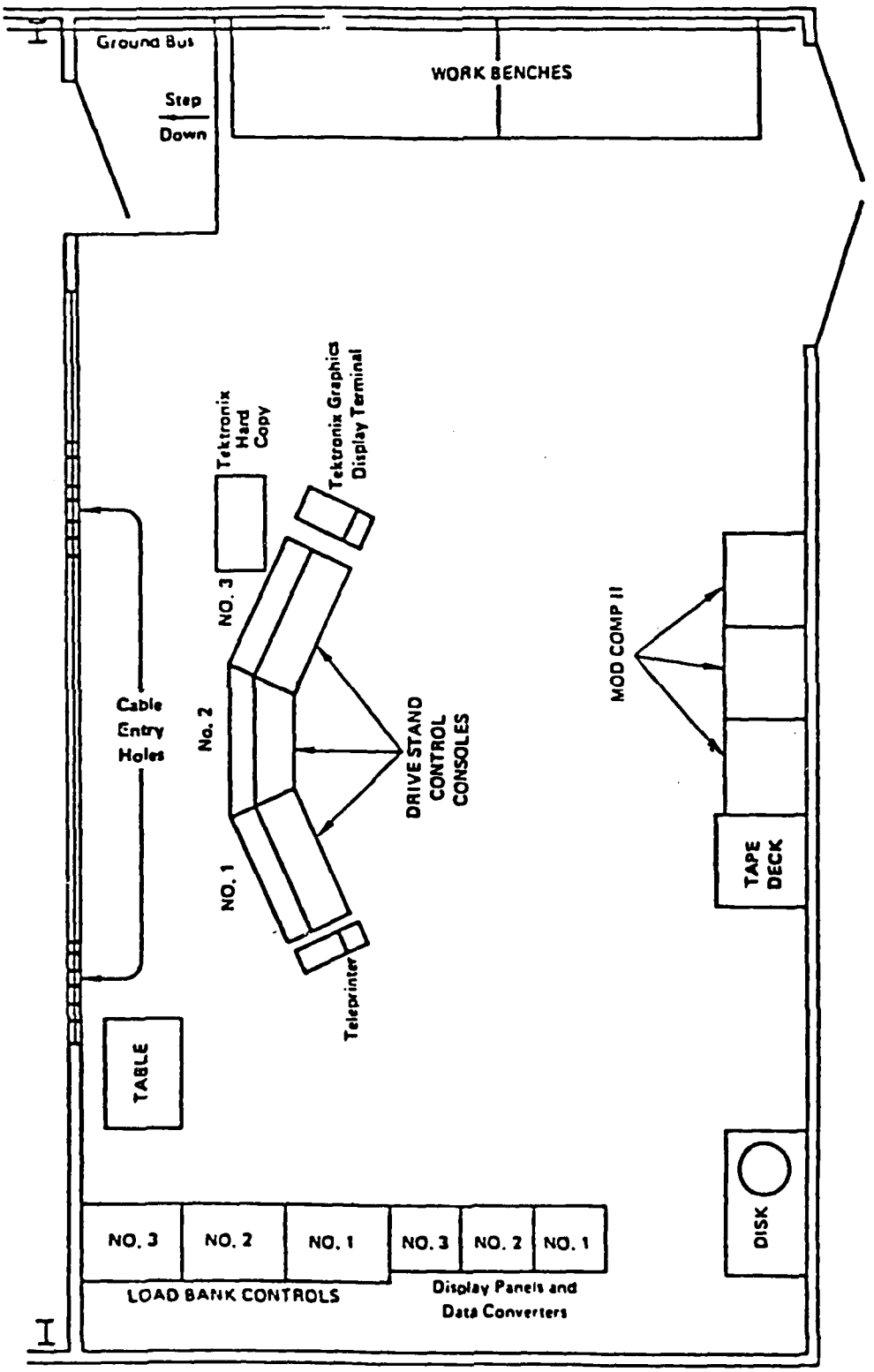


Figure 24 APL Control Room Floor Plan

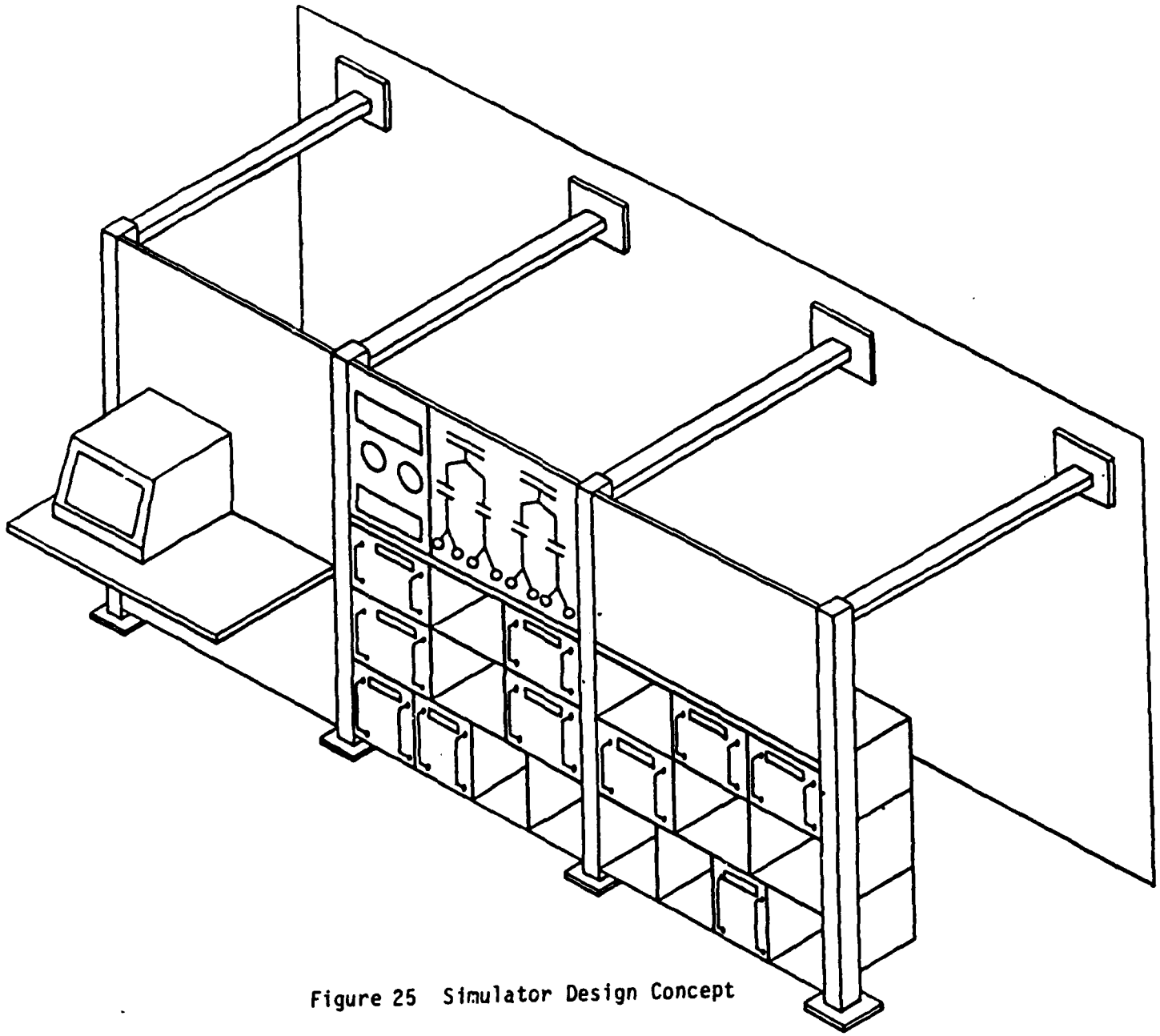


Figure 25 Simulator Design Concept

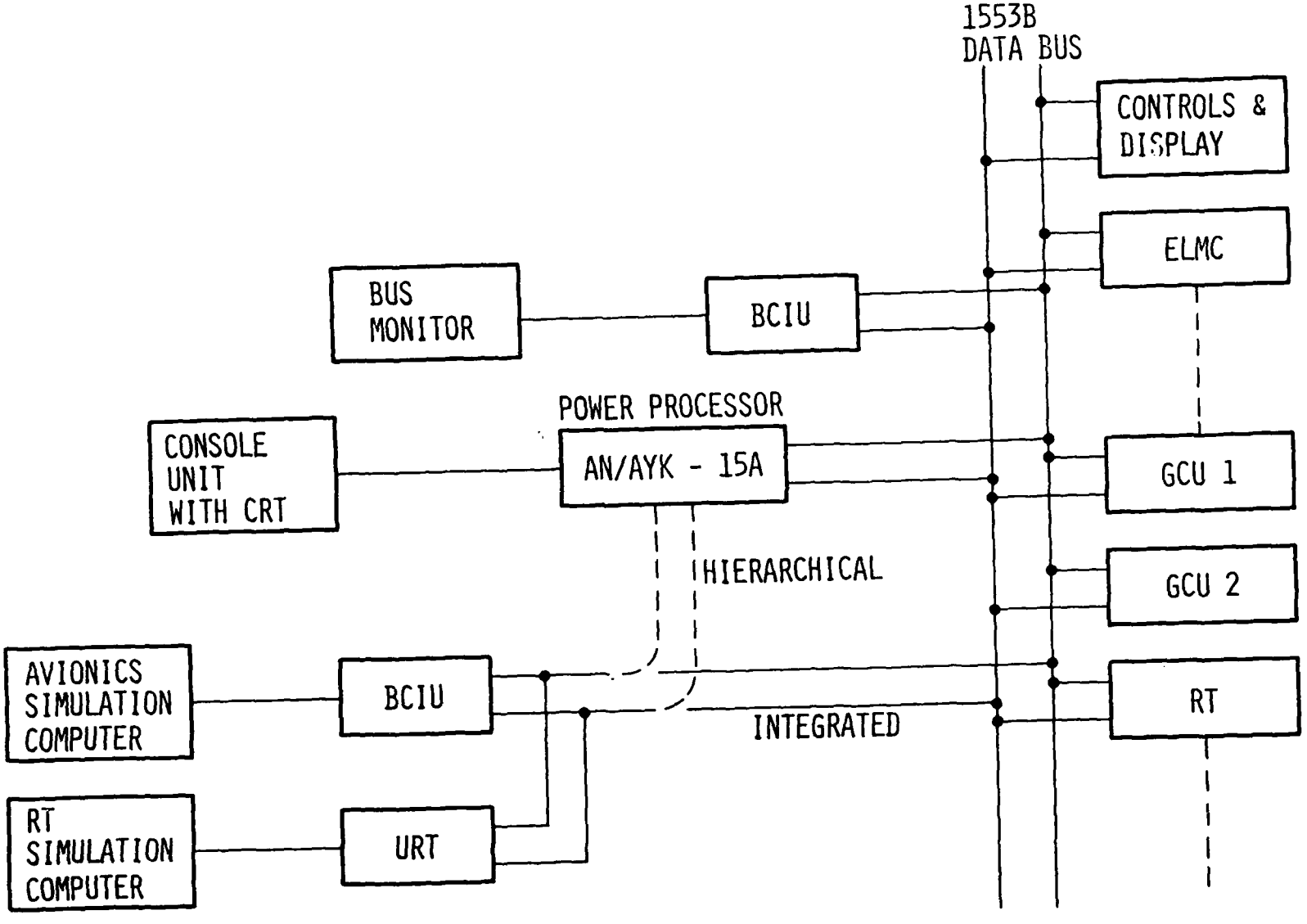


Figure 26 Simulator Block Diagram

is used to record and monitor bus traffic. The console unit with CRT provides the user access into the AN/AYK-15A processor. The bus controller interface units (BCIUs), provide the interface between the 1553B data bus and the support equipment. The universal remote terminal (URT) and the RT simulation computer are used to simulate up to 30 remote terminals on the bus.

The avionics traffic on the data bus is simulated using two computers. The avionics processor bus traffic is simulated with the avionics simulation computer and the BCIU. The bus traffic of the avionics RTs is simulated using the RT simulation computer and the URT. The RT simulation computer can also simulated the bus traffic of the electrical system's RTs, ELMCs, and GCUs. This capability allows experimentation with different hardware complements and configurations without requiring the actual hardware. The simulation computers can also be used to load software into the AN/AYK-15A power system processor.

To support the integrated system architecture, the avionics simulation computer and BCIU, and the RT simulation computer and URT are connected to the 1553B data bus as shown by the solid lines in Figure 26. The dashed-line shows the connection for the hierarchical system architecture. In this case, the power processor becomes an interbus processor. For the non-integrated, dedicated architecture, the avionics simulation computer and the RT simulation computer are not required.

SECTION V
RESULTS AND CONCLUSIONS

The major conclusions resulting from the work conducted during Phase I, Task 1 and 2 are as follows:

1. POWER GENERATION AND DISTRIBUTION

The electrical power system is designed for multi-mission capability. The generator size and number of SSPC's in the system were chosen to support this capability. ELMCs with SSPCs mounted on printed circuit cards were selected. Five ELMCs are required in the system. Each ELMC houses 100 SSPCs. In addition to housing and controlling the SSPCs, the ELMC performs discrete input/output data transfer and analog/digital conversion. The power requirements for the system are met with 2 60KVA main generators and 1 20KVA in-flight operable auxiliary generator. DC power is supplied by 3 100 amp TRUs. Power to flight critical equipment is DC. Flight critical buses are located in the ELMCs and have battery backup power.

The use of J73/I higher order language was evaluated for use in the software development for the electrical system. J73/I was compared with the 1750 assembly language. Two typical power control routines were coded in both J73/I and assembly language. The execution time for assembly language was 10% less than for J73/I; however programmer coding and debugging time was less for J73/I. Execution time was about 10% faster for assembly language. Therefore, it was concluded that J73/I, or its successor J73, higher order language be used instead of assembly language.

2. INTEGRATED POWER SYSTEM CONTROL

In order to meet the processing and data bus loading requirements for a power management system using the DAIS architectural concept, ELMCs containing smart RTs which can process power requests and operate SSPCs are necessary. Even with ELMCs containing smart RTs, the processor loading was greater than 50% for a single power system processor in a hierarchical arrangement. This is due to the additional operating system overhead for interbus communications. This occurs because the processor is both an RT on the avionics bus and bus controller and power manager on the power system data bus.

Because the avionics processor handles the system overhead in the case of the integrated architecture, the power processing requirements can be met by the power system processor. Therefore, the integrated architecture with both an avionics and power system processor sharing a single data bus can meet both processor and data bus traffic requirements. The major assumptions in this conclusion is that the avionics bus load does not exceed 36% including overhead.

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SECTION VI
RECOMMENDATIONS

1. ELECTRICAL POWER GENERATION AND DISTRIBUTION

It is recommended that configuration B, of Figure 6 is used for the preliminary design. This configuration will support a light tactical aircraft with multi-mission capability. The recommended compliment for the distribution system consists of 500 SSPCs, 5 ELMCs, and 3 RTs. In addition, J73 is recommended as the programming language for the software development.

2. DATA BUS ARCHITECTURE

It is recommended that the single integrated data bus architecture shown in Figure 16 with smart ELMCs be adopted for preliminary design of a power management system for a light tactical aircraft. The adoption of this architecture would have the least impact on the current available DAIS concept. Unlike the hierarchical architecture, neither a new processor or a new executive software would be necessary. Both the processor and executive have already been developed and have been thoroughly tested.

The major drawback to the integrated approach is the limitation of 32 elements attached to the data bus and the 1 Megabit/sec data bus traffic rate. However for a light tactical aircraft with smart RTs and ELMCs, local processing capability will keep both the number of elements attached to the data bus and bus traffic to a minimum.

REFERENCES

1. Perry, J. L., Gross, J. P., Hoffman, M. H., "Multiplexing in Aircraft Subsystems," AFAPL-TR-73-41, July 1973.

2. Kevern, G., "Further Evaluation of the Solid State Simulator for the A-7B Aircraft Electrical System," AFAPL-TR-72-88, April 1973.

3. Miller, F., Pico, L., "RPV Electric Power System Study: Phase II," AFAPL-TR-78-93, November 1978.

4. Lautner, D. E., Marek, A. J., Perkins, J. R., "Power System Control Study, Phase I-Integrated Control Techniques," AFAPL-TR-79-2084, October 1979.

5. Edwards, R. J., "Advanced Solid State Power Controller Development, Phase I-Study Report," AFAPL-TR-78-55, September 15, 1978.

6. Caudill, Pat; "Using Assembly Coding to Optimize High-Level Language Programs", Electronics, Vol. 52, No. 3, 1 February 1979, pp. 121-124.

7. Kocher, Christopher P.; "Case of Low-Level Programming", E/E System Engineering Today, Vol. 32, No. 8, August 1973, pp. 81-82.

8. Steele, S.A.; Galbiate, L.J.; "High Order Languaage Evaluation for Real-Time Computer Sytems", Asilomar Conference on Circuits, Systems, and Computers. 7th Annual, November 1973, pp. 471-427.

9. Trainor, W.L.; "Report on High-Order Language (HOL) Standardization for Avionics", Air Force Avionics Lab Wright-Patterson AFB Ohio, AFAL-TR-76-254, January 1977.

10. Trainor, W. Lynn; Burklakoff, Mike; "Jovial-73 Versus Assembly Language -- An Efficiency Comparison", IEEE Procedures National Aerospace Electronics Conference, NAECON 1977 (77CH1203-9), May 1977, p. 502-507.

11. Trainor, W. Lynn; Burlakoff, Mike; Garrett, John; "Efficiency Comparison of Jovial-73/I and AN/AKY-15 Assembly Langauge", Air Force Avionics Lab Wright-Patterson AFB Ohio, AFAL-TR-76-253, January 1977.

12. Wickham, K., "Pascal is a Natural (for Microprocessor Software Programs)", IEEE Spectrum (USA), Vol. 16, No. 3, March 1979, pp. 35-41.

13. Yourdon, Edward; Constantine, Larry L.; Structured Design; Fundamentals of a Discipline of Computer Program and Systems Design, 1978 Yourdon Inc. New York, pp. 3-14.

14. System Specification For The Digital Avionics Information System, SA120 100, SCN#1 11 Jan 80, AFAL, WPAFB.

15. B-1 EMUX Specification L409C2008, Code identification #43999, Rockwell International B-1 Division.

16. System Development Manual for the AN/AYK-15A Processor, 80-D141A, System Development Division, Westinghouse Corporation.

17. Time Item Development Specification for AN/AYK-15A Digital Processor, Part I, Type B-1, DAIS library #SA-421205, 1-APR-79.

APPENDIX A

PROCESSOR LOADING CALCULATION TECHNIQUE

Shown here are the steps involved for calculating the processor loading of the power processor in a integrated - dumb RT configuration.

1) the time required for the processor to calculate each type of equation was accurately measured by coding the equation and adding the execution times of the instructions produced by the compilation.

   the total time required to execute all equations, by category, is as follows:

category I :	30199 usec
category II :	19000 usec
category III:	17000 usec
	66199 usec

2) 5% of the processing is divided over 2 minor cycles to meet the 50 msec response time.

   95% of the processing is divided over 32 minor cycles to meet the 300 msec response time

(.05)	(66199)	2 =	1655 usec
(.95)	(66199)	32 =	1965 usec
			3620 usec

   this total is divided by the length of a minor cycle to get the processor loading percentage for equations only.

   (3620/7812.5) x 100 = 46%

APPENDIX B

BUS LOADING CALCULATION TECHNIQUE

Shown here are the steps involved (with explanations) for calculating the bus loading of a integrated - dumb RT configuration.

1) the bus loading calculation begins with a description of the number of discrete bits to be transmitted in and out of each device as noted in the following table:

DEVICE	IN	OUT
ELMC1	250	118
ELMC2	250	118
RT1	167	118
GCU1	50	50
ELMC3	250	118
ELMC4	250	118
ELMC5	250	118
RT2	167	118
GCU2	50	50
RT3	167	118

2) one assumption of the bus loading analysis is that the 5%/95% response distribution is evenly divided across all I/O as noted in the following table.

	5 devices @ 250 bits	3 devices @ 167 bits	2 devices @ 50 bits	8 devices @ 118 bits	2 devices @ 50 bits
5%	13 bits	8 bits	3 bits	6 bits	3 bits
95%	237 bits	159 bits	47 bits	112 bits	47 bits

this table states that 5 devices will receive 13 bits at one rate and 237 bits at a (presumably slower) second rate.

3) a second assumption used in the bus loading analysis is that bata bits are packed a maximum of 12 data bits in a 16 bit word. The bit totals from (2) above are divided by 12 to get the number of words per message.

BITS	=	WORDS	
13		2	5 devices send/or review this message
8		1	3 devices send/or review this message
3		1	2 devices send/or review this message
6		1	8 devices send/or review this message
3		1	2 devices send/or review this message
237		20	5 devices send/or review this message
159		13	3 devices send/or review this message
47		4	2 devices send/or review this message
112		10	8 devices send/or review this message
47		4	2 devices send/or review this message

therefore, there are:

15	1 word messages
5	20 word messages
3	13 word messages
8	10 word messages
5	2 word messages
2	4 word messages

this is all messages required for all I/O.

4) the time required to send a single bus message is calculated as follows:

time = (T (NW + OV) + RT + GT)

where:

T is time required for one word to be sent on bus. on a 1 MHz bus, this is 20 usec.

NW is the number of words in the message

OV is the number of overhead word. for 1553B this is equal to 2 words.

RT is the response time which is the time required for the device to response to the bus command. for 1553B this is 8 usec

GT is the gap time which its the time lapse between bus messages.

example: how much time is required to send a 12 word message?

time = (20 usec(12 + 2) + 8 usec + 4 usec)

time = 292 usec

5) the time required to transmit the deviced set of bus messages is now calculated as follows:

15	1 word messages	=	15	(20(1 + 2) + 8 + 4)	=	1080 usec
5	20 word messages	=	5	(20(20+ 2) + 8 + 4)	=	2260
3	13 word messages	=	3	(13(12+ 2) + 8 + 4)	=	582
8	10 word messages	=	8	(20(10+ 2) + 8 + 4)	=	2016
5	2 word messages	=	5	(20(2 + 2) + 8 + 4)	=	460
2	4 word messages	=	2	(20(4 + 2) + 8 + 4)	=	264

6) all of the 1 and 2 word messages represent the 5% distribution and are divided over 2 minor cycles to meet the 50 msec response time.

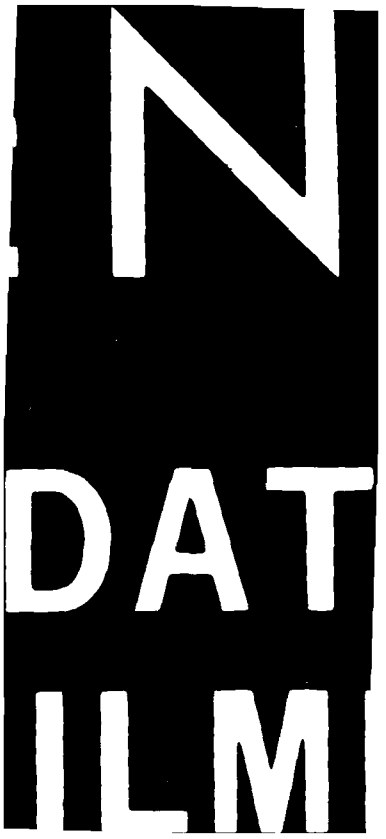
all of the other message represent the 95% distribution and are divided over 4 minor cycles to meet the 300 msec response time.

460/2	=	720
1080/2	=	540
2260/4	=	565
582/4	=	146
2016/4	=	504
264/4	=	66
		2051 usec

the result is divided by the length of a minor cycle to get the bus loading percentage:

2170/7812.5 = 26%

add to this the avionics load to get total bus loading.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